Signal Integrity Verification for On-Chip Long Interconnect Lines

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Sumario

Los circuitos integrados (CIs) que son fabricados con tecnolog´ias actuales presentan estructuras complejas. CIs actuales pueden contener una gran cantidad de sistemas. Estos sistemas trabajando en conjunto logran realizar la función o funciones para que fue diseñado el CI. El CI con estas características es llamado SoC (por sus siglas en inglés). Estos tipos de circuitos son el resultado de la gran capacidad de integración que permiten las tecnologías actuales. Varios millones de transistores pueden ser agrupados dentro de un CI. Esto aumenta considerablemente la densidad de líneas de interconexión necesarias dentro del CI.

Las líneas de interconexión pueden transportar señales con frecuencias en el rango de los gigahertz. La alta densidad de estas líneas de interconexión y señales viajando a altas frequencias hacen que el acoplamiento entre líneas tengan un impacto importante en la integridad de la señal que viaje por las líneas de interconexón.
Es importante conocer los problemas de integridad que pueden presentar las señales que viajan dentro del chip. Esto permitirá establecer técnicas de verficación que ayuden a saber cuando una señal no tiene los niveles adecuados de integridad.

La tesis esta organizada de la siguiente manera:

El Capítulo 1 da una introducción al estado del arte del diseño electrónico actual y los problemas que se surgen al utilizar tecnologías nanométricas. Algunos trabajos relacionados con la verificación de integridad de señal son presentados.

El capitulo 2 presenta un análisis the la integridad de la señal en líneas

de interconexion. El caso de implementar líneas de protección en un bus de datos para reducir los efectos de acoplamiento capacitivos e inductivos es presentado y analizado. En este capítulo se presenta una metodología para analizar el impacto de las líneas de protección en la integridad de la señal cuando estas presentan un defecto.

El Capítulo 3 presenta una nueva metodología de verificación de integridad de señal. Dos monitores son utilizados para detectar violaciones de integridad de la señal en los estados lógicos alto y bajo de una señal digital. Es posible mediante esta metodología verificar más de dos señales con solo dos monitores.

El Capítulo 4 muestra los resultados experimentales obtenidos mediante las mediciones realizadas al circuito integrado diseñado y fabricado. Diversas mediciones son realizadas para mostrar el buen funcionamiento de la metodologia propuesta.

En el Capítulo 5 se presentan las conclusiones de la tesis.

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Dedicates

Quiero dedicar esta tesis esta a :

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Preface

The integrated circuits (ICs) fabricated with current technologies are complex. These ICs can implement several systems to achieve a specific function or functions. This type of ICs is called system on chip (SoC). This feature of the current ICs is due to the nanometric technologies that allows to integrate millions of transistors into a single chip. A large variety of design possibilities is given with these technologies to implement analogue and mixed-signal circuits in the same substrate.
Microprocessors, for example, can be combined with high precision digital to analogue and analogue to digital converter in the same chip. This allows to save manufacturing cost, because the chip to chip interconnections are reduced. However, the amount of implemented transistors and on-chip interconnects is increased with these nanometric technologies. Also each new scaled technology allow to increase the frequency performance of the implemented circuitry. These characteristics, the high density of on-chip interconnects, transistors and high rates of switching activity generate several new issues in current integrated circuits. An important issue is the signal integrity degradation due to capacitive and inductive coupling between interconnects, the electromagnetic effects generated at high frequencies, process variation, and manufacturing defects

A current design challenge is to assure acceptable signal integrity levels in order to have the correct performance of the overall system. Because of this, signal integrity verification is important to advise if violations of the signal integrity occur in the implemented systems. The effort of the verification techniques is addressed for solving the issues like signal skew, jitter, ringings, etc. The scope of this work is to analyze and present a methodology for signal integrity violation in interconnects, and to propose a verification technique in order to detect the unacceptable ringing in high speed digital signals. The

thesis is organized as follows:

Chapter 1 gives an introduction of the current state of the art of the electronic design and the issues generated by using nanometric technologies. Some works related to signal integrity verification are presented

Chapter 2 analyze the signal integrity in interconnects. The performance at high frequencies of these interconnects are obtained by simulation. The case of implementing shielding lines in a bus structure is also analyzed. A methodology to analyze the impact of shielding line defects over the signal integrity is proposed.

Chapter 3 proposes a novel signal integrity verification methodology. High speed signals are verified by using two monitors. Undershoots in the high logic levels and overshoots in the low logic level are sensed by the high and low level monitor respectively. The methodology uses a coherent sampling scheme to capture the signal information. A complete scheme to verify more than two signals is also presented.

Chapter 4 presents the experimental results obtained for designed and fabricated circuits. Several measurement are made in order to show the feasibility of the proposed methodology.

Chapter 5 gives the conclusion of the work. The obtained results and contribution of the thesis are presented.

Acronyms

ADC	Analog to Digital Converter
ATE	Automatic Test Equipment
CAD	Computer Aided Design
CDF	Commulative Distribution Function
DAC	Digital to Analog Converter
DFT	Design For Test
FFT	Fast Fourier Transform
HSB	High Significant Bit
I/O	Input/Output
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
LSB	Low Significant Bit
MNA	Modified Nodal Analysis
NH	Noise Heigh
NW	Noise Width
OD	Overshoot Detector
PEEC	Partial Element Equivalent Circuit
PLL	Phase Locked Loop
RF	Radio Frequency
SI	Signal Integrity
SIV	Signal Integrity Violation
SoC	System on Chip
SUV	Signal Under Verification
UTP	Unit Test Period
VCO	Voltage Controlled Oscilator
VLSI	Very Large Scale Integrated

Chapter 1

Introduction

During the last decades the growing of the electronic industry has been based in the evolution of the semiconductor technology. Technologies have been scaled down according to the Moore law [1] [2]. This has allowed improvements in cost per function and performance. The increasing clock rate and SoC integration presents severe challenges in the design and test of current complex integrated circuits [3]. Due to this, the designer needs to prevent new problems like crosstalk noise, substrate noise, power supply drop, etc [4]. All these factors can affect the signal integrity and may produce an unreliable performance of the system. Many of these new issues appearing in modern technologies can be solved if proper testability and DFT strategies are considered and incorporated early in the design phase. However, some of these problems may remain and appear during the field application. This is because is not possible to take into account all the possible environmental and required signal combinations during the design phase. Hence, verification methodologies for identifying these problems before delivering the product to the customer are required.

Verification of signal integrity requires testers at the GHz range which are expensive. Furthermore, external speed verification is not possible for the newest technologies. Due to this built-in verification strategies appear as a good alternative for current nanometer technologies.

The first section of chapter presents the performance of current electronic systems. The characteristics, emerging issues and challenges for this actual systems are presented. The issue of testing for these systems is explained

next. Then, the signal integrity concern is presented. Next section shows the related work of signal integrity verification. Finally, the last section presents the organization of this thesis.

1.1 Performance of actual electronic systems

Design technology is the discipline that transforms the project ideas of the electronic designers into manufactured and testable representations [1]. Designers need several elements in order to make real their ideas. Those elements like *tools, libraries, manufacturing process characteristics, and methodologies* help the designer to get the *conception, implementation, and validation* of microelectronics-based systems. Furthermore a better understanding of the relationship between electronic science and physical science is required.

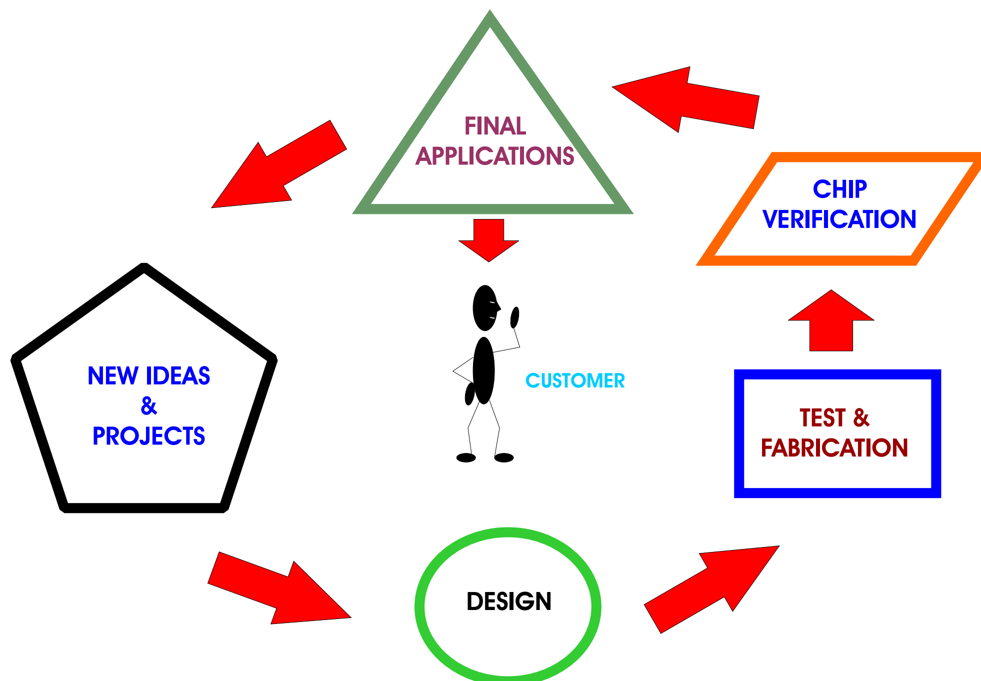

Figure 1.1: Ideas and objectives are transformed in electronic applications

For instance, the theories of electron devices and circuits components are built on principles of solid-state physics, statistical mechanics, and thermodynamics [5]. Nowadays, the traditional circuit theory is not adequate to deal with the many complex problems that have emerged since the advent of the Very Large Scale Integrated (VLSI) circuits. In VLSI systems it is found a big number of active devices and interconnects where their components interact

strongly with each other. In this case, the traditional circuit theory is unable to manipulate, in a adequately way, the analysis. In these cases, numerical analysis is effective to predict the behavior of well-specified circuits with the parameters values specified, but it provides no general understanding of the circuits. Often, interpretation of the simulation results is the hardest part of the circuit design verification. All the previously mentioned factors are important issues in current high performance integrated circuits [5] [6] [7].

The principal actor in these current circuits is the transistor. The transistors fabricated with actual technologies have features sizes (channel widths and lengths) in the range of nanometers. Transistors with these features may turn-on or turn-off at very short times. Because this, the frequency performance of the circuits designed with these transistors can get high rates. The roadmap for feature sizes (gate length) from the year 2003 to the year 2018 is presented in Fig. 1.2 [1].

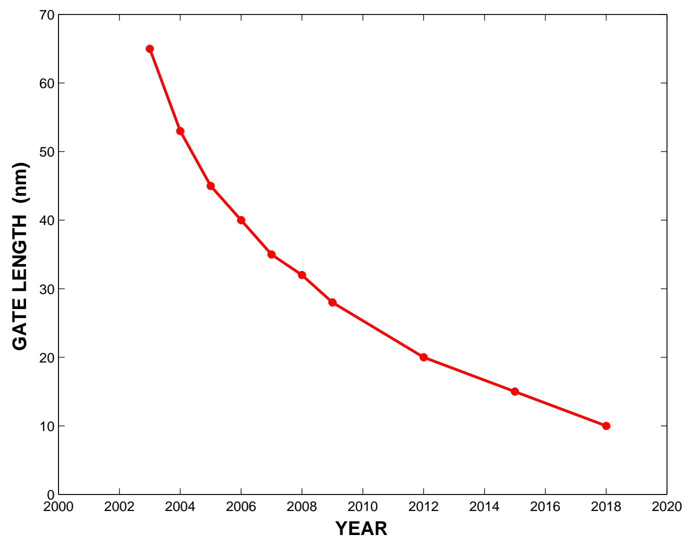

Figure 1.2: Road-map of the transistor gate length trough the years. Data taken of the ITRS 2004.

The integration capacity in current technologies allows to have millions of transistors in a single chip [8] [9]. Complete systems can be implemented

in these chips. The circuits implementing systems in a single die are called System on Chips (SoCs). In this approach, a set of circuits is used to perform a specific function or functions into of a digital or analogue core, and a set of cores into a single chip builds the so called SoCs. Fig. 1.3 shows a SoC built with several cores.

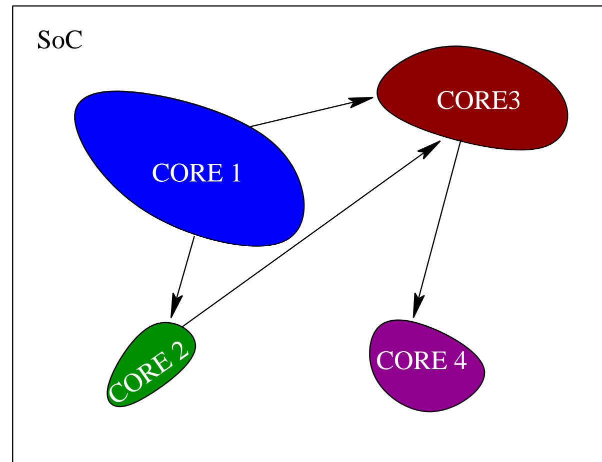

Figure 1.3: Several cores are used to make a system on chip (SoC).

The SoC implementation and new technologies arise design complexities [1]: *Silicon complexity* and *system complexity* (see Fig. 1.4).
The first one refers to the impact of process scaling and the introduction of new materials or device and interconnect architectures. The second one refers to exponentially increasing amount of transistors in a single chip. Because silicon complexity, several previously ignored phenomena are currently becoming of quite importance in new technologies [8] [5]. As indicated by International Technology Roadmap for Semiconductors in [1], the predominant sub-micron effects are:

- non-ideal scaling of device parasitics, supply and threshold voltages,
- coupled high-frequency devices and interconnects,
- manufacturing variability
- scaling global interconnect performance relative to device performance (communication, synchronization)

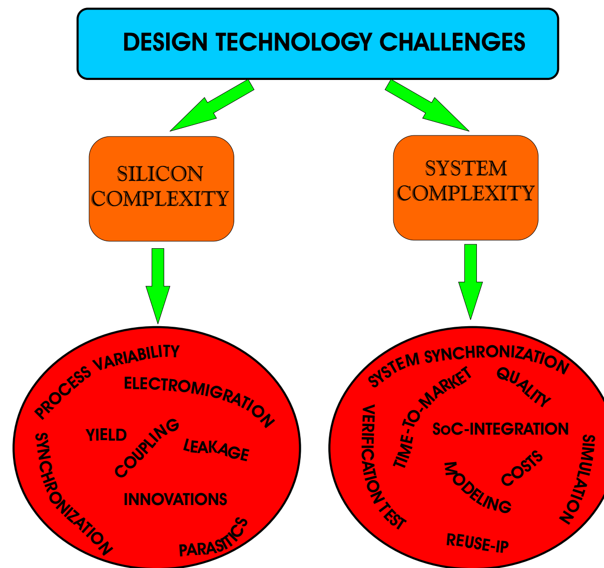

Figure 1.4: Complexities and challenges for current design technologies

- decreased reliability (gate insulator tunneling and breakdown integrity, electro-migration, general fault tolerance)
- complexity of manufacturing hand-off (reticle enhancement and mask writing/inspection flow)

In system complexity, the higher integration of devices is due to the smaller features sizes and spurred by consumer demand for increased functionality, lower cost, and shorter time-to-market. Design specification and validation become extremely challenging, particularly with respect to complex operating context. Trade-off must be made between all aspects of value or quality, and all aspects of cost. Implied challenges include:

- reuse (modeling, simulation, verification, test of component blocks)
- verification and test
- design process management (design team size and geographic distribution, data management, collaborative design support, metrics and continuous process improvement)

The acknowledge of the additional considerations such as design reuse and manufactured system cost in the design optimization must be shared [5] [1]

[10]. Together, the silicon and system complexity challenges imply exponentially increasing complexity of the design process. In order to deal with this complexity, design technology must in general provide optimization and analysis of more complex objectives and constrains.

1.2 Testing of high performance circuits

The task to inspect the correct circuit performance falls in the test discipline [11] [12]. A lot of work to test different type of faults has been developed for many years. With the advent of the nanometric technologies, the test has increased in complexity. Nanometric technologies allow to integrate millions of logic gates in a single chip, thousand of external pins, and clock rates of the order of gigahertz. Chips with these features make difficult the task of the test. Test cost per unit and test equipment capital cost consideration continue to dominate test methodology decisions. Design for test (DFT) methodologies have contributed to reduce the cost of the test equipment [13]. However, this cost continue being significant [1] [14]. Fig. 1.5 shows, as example, the number of automatic test equipment (ATE) channels and the cost per channel for different kind of tests. This example is for ASIC-microprocessors using functional, structural and memory test. The total test cost is given by the cost per channel and the cost for the number of channels plus the base cost.The base cost include the mechanical infrastructure, black-plane, central instruments, and other resources. The base cost for the ASIC-microprocessors is in the order of $250K - $550K [1]. If the system complexity continues growing as expected, the ATE would require more pins to test the system, hence the test cost is also increased. Systems-on-Chip (SOC) designs are breaking the traditional barriers between digital, analog, RF, and mixed-signal test equipment capability requirements, resulting in a trend toward highly configurable, one-platform-fits-all test solution [5] [15]. A different approach is clearly needed.

Test automatization is required for the semiconductor industry in order to continue producing faster, smaller and powerful commercially viable chips. One approach to counteract these issues is given by implementing test circuits onto the chip. This means making more use of DFT techniques. The basic idea of the DFT is to identify key internal nodes and to implement the required structures to make those nodes accessible from outside the chip.

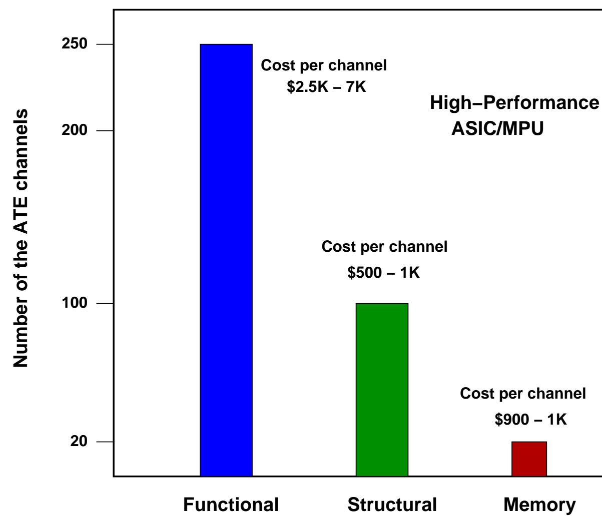

Figure 1.5: Number of the ATE channels required to accomplish three different kind of test to the ASIC microprocessors [1].

The goal for using any DFT technique is to achieve the detection of the highest number of potential faults. It means, to increase as much as possible the fault coverage. DFT-based test approaches require continue research to increase coverage of actual process defects through development of advanced and feasible test methodologies. It is expected that DFT technologies will continue to lag leading-edge device performance and complexity.

At-speed functional test has provided a robust methodology for high volume manufacturing for many years. The use of this methodology has allowed to achieve high quality levels [16] [17]. It can be argued that this method is reaching its limits for several reasons, such as test development resources, manufacturing yield loss, and cost [18] [19]. Even if there is an affordable process to upgrade or replace manufacturing test equipment as the device performance improves with each scaled technology. It has been proved to be impossible to avoid the resource requirement for manual test writing in the functional test environment. Test content generation may require tens of person years for highly complex designs [1] [20]. DFT techniques like scan and Built-in-Self Test (BIST) either enable test content to be generated automatically or reduce the test content generation effort. Hence, it reduces drastically the manual test writing task. For highly complex integrated de-

vices, DFT is required to provide re-use test collateral and avoid a geometric or exponential growth of the test development and validation effort [21] [5] [20].

An important emerging issue in nanometric technologies is signal integrity. Capacitance coupling between interconnects, large number of interconnects and gigahertz frequencies are determinant factors which affect the performance and reliability of high performance SoCs [2] [14] [8]. On-chip signal integrity verification is required in order to assure the correct performance of the entire chip [22] [23].
In the next section, the signal integrity issue is analyzed.

1.3 Signal integrity issue

High speed electronics operates actually in a ultra-wide frequency band up to several tens of gigahertz. At these frequencies, several electromagnetic effects can produce signal integrity degradation [24] [25] [26] [27]. Signal integrity violation (SIV) can be produced by several sources of noise. Substrate noise is an important issue because it can affect noise-sensitive circuitries such as analog blocks. When a digital block switch, current is injected toward substrate by coupling of the interconnects and devices. This substrate current may cause interference or a faulty behavior of a sensitive circuit near to the digital block. Another problem is due to large power nets and long interconnects that cause power supply drops. Current technologies permit to integrate an increasing number of devices onto a chip. The large amount of devices connected to the power supply net increases the current consumption at different points of the net. Localized drops of the V_{DD} level are difficult to predict. The performance of the system is affected by increased delay and reduction of noise margin.

Interconnects play a major role in signal integrity, hence, they significantly impact the system performance. The current and future design challenge of the SoCs are to connect efficiently the core components into a reliable network in order to perform the desired functions. Because of this, it is possible to have on-chip micro-networks [28] [29]. In general the communications between cores into the SoC may present errors due to technology factors like voltage ringings. Other factors are electromagnetic interference as well

as capacitive and inductive crosstalk. Long interconnects running close to each other present a significant coupling capacitance. This is because the lateral capacitance is quite important in actual integrated circuits [30] [31]. Furthermore, in high performance systems the inductive coupling between interconnects becomes significant and the total inductance of the interconnect should be taken into account [32].

Signal current variations on an interconnect generates a variable magnetic field. This magnetic flux ($\vec{B}$) creates an electric field $\overline{E}$ and this $\overline{E}$ generates, on near loops, inductive voltage noise as show in Fig. 1.6. Levels of crosstalk noise depend on the coupling capacitance/inductance between interconnects, the total resistance and capacitance of interconnect and the driver strengths of the aggressor and victim lines. The distributions of the

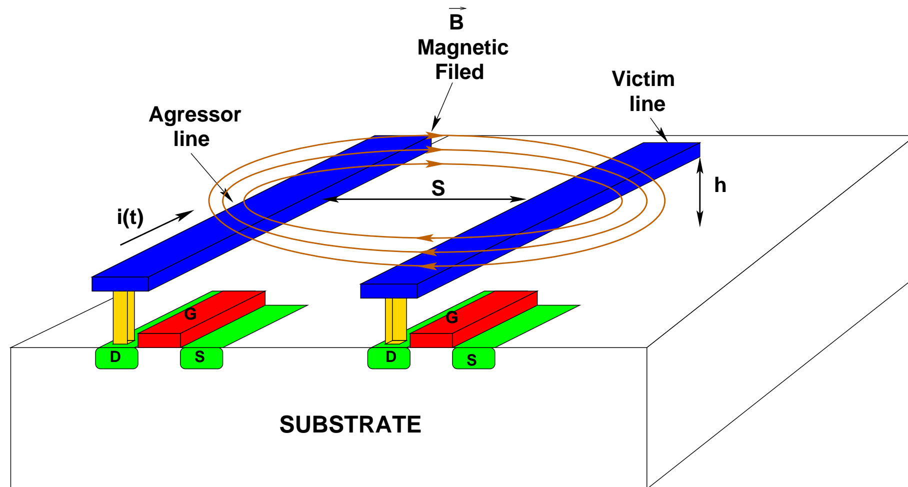

Figure 1.6: A changing magnetic field due to a current variation through to the interconnect cause a induced voltage in a near interconnect.

electromagnetic fields depend on the logic blocks and interconnects physical distribution. Furthermore, they also depend on the switching activity of the signals traveling across them. The integrity features of the signals traveling across interconnects have an strong dependence on the switching activity of the input signals.

Because current technologies allow to integrate more and more coupled interconnects, the higher switching speeds of the signals cause many integrity

problems. The dependency of the signal integrity characteristics on the switching activity is needed to be taken into account for the signal integrity verification of the circuit performance [33] [23]. In coupled lines, the signal propagation delay could vary 50% of the propagation delay of a single isolated line with the same physical structure [33].

The coupling influence in critical signals is addressed by inserting shields between interconnects. These shields are additional V_{DD} and GND wires which typically are inserted between critical global interconnects. The capacitive coupling is almost eliminated by the shield wire. Also the self-inductance of the wire is reduced by the shield wire because the electric field return path around the interconnect is provided very close to the line. The shield wire also limits the inductive coupling between interconnects on either side of the shield wire by reducing the electric field [33][34].

With a great number of critical interconnects switching at very fast frequencies, the number of the shielding wires is increased in order to reduce the capacitive and inductive coupling. The effective capacitance and inductance of the interconnect is determined by the switching activity and not only by the physical features. The shielding wires can be switched in order to reduce the return path of the electric field (loop inductance) and the delay by the capacitive coupling [35] [36]. The recommended ratio between the signal and shield wire is 2:1 for the design of high performance processors [37] [27]. The connections of the shielding lines to ground could present resistive open defects [38]. A resistive open appears when the conductive material is not completely broken. This defect indirectly affects the integrity of the signal traveling on adjacent signal lines. Ringing values of the signal could vary significantly. Hence, a faulty behavior of the system can occur [35] [34].

Characteristics of interconnects as narrow width, closeness of the wiring, etc., affect directly the SI [30] [34]. To ensure SI, designers need to consider circuit design, placement and routing, and circuit simulation. Current tools could help the designer in all these tasks. A good approach in order to minimize noise level is to be careful and methodical in circuit simulation [6]. The problem is that all possible environmental and signal combinations are unlikely to be taken into account in the simulation. Consequently practical experience shows SI violations not foreseen by the present state of the art CAD tools. Verification of critical signals would require testers at GHz range

which are expensive. Furthermore, external at-speed verification may not be possible for newest technologies. Due to this built-in verification appears as a good alternative. This strategy also allows to verify some internal nodes difficult to control or to observe at the I/O pins.
In the next section, several related works to signal integrity verification are shown.

1.4 Related signal integrity verification techniques

As explained before, signal integrity is an important issue in actual high performance circuits. Also the interconnect effects play an important role in the signal integrity verification (SIV) of high speed signals. Several studies for interconnect impact on circuit performance can be found in [34] [39] [32] [33] [37] [2]. Several crosstalk defect-oriented analysis solutions have been developed on multiple-coupled interconnects. The work presented in [40] shows a crosstalk-defect simulation methodology. This approach allows a fast analysis for interconnects dominated by capacitive coupling and estimate the noise effects based in the interconnect signal transitions. Other analysis about the crosstalk and their impact in signal integrity can be found in [41] [23] [42] [43].

Problems such as skew and jitter are present in actual SoCs structures where sets of long interconnects are present. Some studies of these problems can be found in [44] [45] [21]. The authors in [46] present a test pattern generation algorithm for signal integrity faults on long interconnects. In this approach it is possible to detect intermittent failures due to integrity loss on long interconnects.

In [47] the authors presents a sense amplifier for detecting small delay variation between two signals. In [48] the authors present on-chip mechanisms including testing of interconnects for signal integrity by extending the JTAG standard, but they did not include the effect of mutual inductance and their sensor is noise-sensitive. Another important contribution is given in [49] where cells to detect noise and skew are presented. However, one sensor per cell is required to verify each critical signal, which penalizes the area. In the approach presented in [50], the authors propose a frequency-based

technique for measurement jitter. They analyze sampled data at low frequency and shift the data into a tester using software-based analysis. This technique coherently under-sample a received signal by clocking the receiver at a frequency slightly lower (beat frequency) than the transmitted data frequency (see Fig. 1.7). The output of the latch is a synchronous data

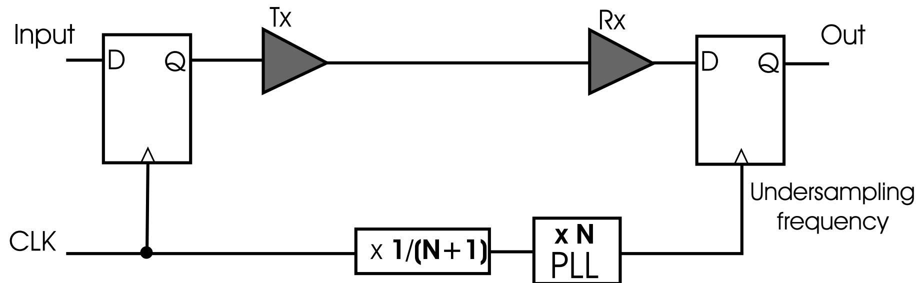

Figure 1.7: Jitter measurement technique using coherent under-sampling.

stream that can be deserialized and analyzed on-chip at low frequency using software-based analysis. The technique focus on the unstable bits in the output caused by rising/falling-edge jitter to measure the statistical properties of the jitter. By having groups of these unstable bits the authors derive a cumulative distribution function (CDF) and from these CDF they derive a jitter histogram. The drawback of this approach is that the technique need to generate an under-sampling frequency just slightly lower than the system high speed clock, this is still a high frequency signal for clock speeds at rates of gigahertz. An interesting work about testing overshoots can be found in [51]. The authors present a CMOS overshoot detector (OD) cell, which consists of a modified cross-coupled PMOS differential sense amplifier for detecting voltage overshoots in bus lines. Fig. 1.8 shows the detector cell.

Their OD cell sits physically near the receiving core and observe the actual signal plus noise received by core B (see Fig. 1.8). The output stored in the OD cell is analyzed by a DFT decision. Three choices to transfer the information to the output are presented. One of them is by using a compressor to compact the information given by the OD cell. Then the information can be sent-out through scan registers. Another way is recording the occurrence of overshoots in flip-flops. The information is also scanned-out. The last option given by authors is using a counter for collecting information of overshoots occurrence. The outputs of the OD cells are connected to a n-input

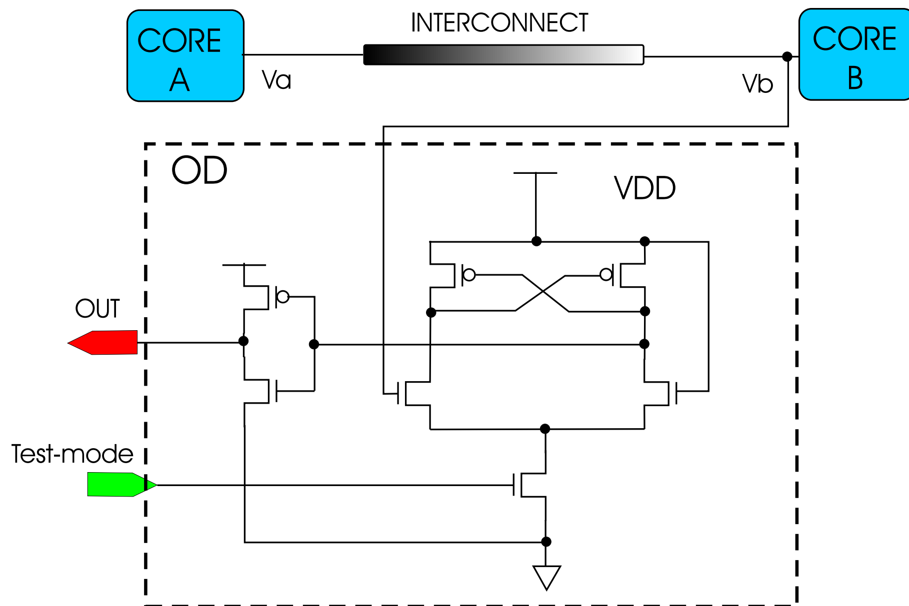

Figure 1.8: Overshoots testing: A CMOS cross-coupled sense amplifier.

NAND gate, which output will be **1** if at least one overshoot occurs (the output of the OD cell is **0** if a overshoot occurs). The output of the NAND gate is connected to the clock line of a counter to record the number of times that the core input is exposed to overshoots. This proposal is efficient for testing the occurrence of voltage value above V_{DD} (overshoots) in a bus system, but it is not able to sense ringing or undershoots.

1.5 Organization of the thesis

The rest of the document is organized as follows: The chapter 2 shows the interconnect modeling and an approach to establish the integrity features of the interconnect for several lengths. The performance at high frequencies of interconnects are obtained by simulation. The impact of shielding lines to reduce the crosstalk in a bus structure is also analyzed. A methodology to analyze the effects of shielding line defects over the signal integrity is proposed.

A novel signal integrity verification methodology is proposed in chapter 3. Digital signals are verified by using two monitors. Undershoots in the high logic levels and overshoots in the low logic level are sensed by the high and low level monitor respectively. The methodology uses a coherent sampling scheme to capture the signal information. A complete scheme to verify more than two signals is also presented. A control circuitry to verify several signals under the sampling scheme is proposed

Chapter 4 presents the experimental results obtained measuring the performance of the designed and fabricated signal integrity monitors. Also, the coherent sampling scheme applied with the proposed monitors has been validated.

Finally, the conclusions of the thesis are given in chapter 5. The contributions of the thesis work are discussed in this chapter. Also, the constraints and future work are presented in this chapter.

Chapter 2

Interconnect characterization and signal integrity loss

Interconnect structures in high speed circuits play an important role in present and future CMOS technologies. Inductance and capacitance coupling effects (crosstalk) may cause significant loss in signal integrity in high performance systems. One way to reduce these effects is to place a signal line between two grounded lines (shield). The shielding lines are connected to ground from the metal wire to the substrate through vias. In this chapter we study the influence of defective grounding of shielding lines. We focus on resistive open defects due to manufacturing problems or broken vias. Faulty shields may cause undershoots or ringings in signal traveling in long interconnect lines. An analysis of the interconnect behavior in the presence of a resistive open has been performed using a lumped RLC circuit in one, two, three stages and compared with the interconnect Hspice model. Simple expressions for undershoots and overshoots have been derived using dominant poles to determine the zones of signal integrity violation for different lengths of interconnect lines. The results show the impact of defective grounded shields.

The chapter is organized as follows: In section 2.1, the coupling between interconnects is analyzed. Section 2.2 shows the simple equations from a lumped RLC circuit. These equations help to achieve overshoot and undershoot expressions. Also, a comparison of the root loci for one, two, and three lumped stages is made in this section. Shielding strategies for reducing induced voltage noise are discussed in section 2.3. Section 2.4 shows some

aspects of signal quality. Ringing and undershoot values are characterized for different lengths of interconnects with open shield defects. Regions for acceptable and non-acceptable signal integrity levels are established in section 2.5. Finally, conclusions are given in section 2.6.

2.1 Coupling between interconnects

In deep-submicron technologies the on-chip wire density is very high. Current interconnect features allows to implement wires nearest to each others. Each wire is electrostatically coupled with its closest neighbors [52] [53]. Fig. 2.1 shows the coupling cases of on-chip wires. When scaling all dimensions, the capacitance per unit length among the wires remains unchanged. This is true if the wire thicknesses is also scaled. If the scaling factor is S, the resistance per unit length is increased by a factor of $1/S^2$. This means that the constant RC is increased due to dimension scaling [54] [55] [56] [57].

If the wires spacing is comparable with the metal thickness, the coupling

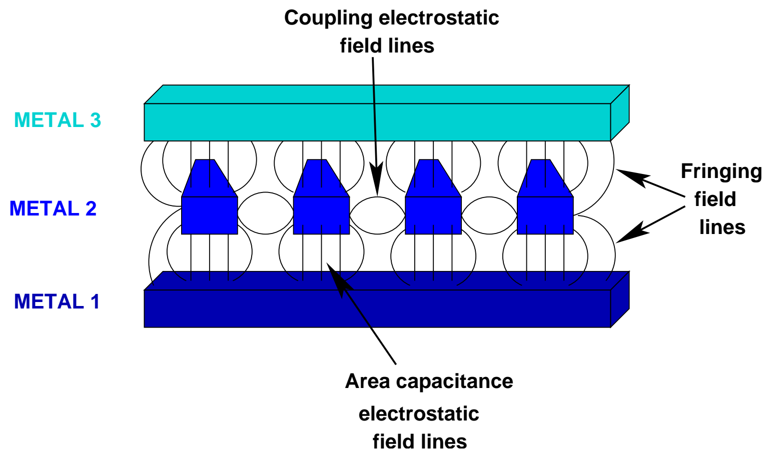

Figure 2.1: Coupling features of the alternated in direction metal interconnects. The physical localization and the shape of the interconnects generate the coupling, fringing and area capacitance

capacitance between wires has a considerable value [34]. Fig. 2.2 shows graphically this phenomenon. Because this, it is important to take into account the coupling capacitance between interconnects and its impact in the

signal integrity. Faster switching signals require interconnects with lower re-

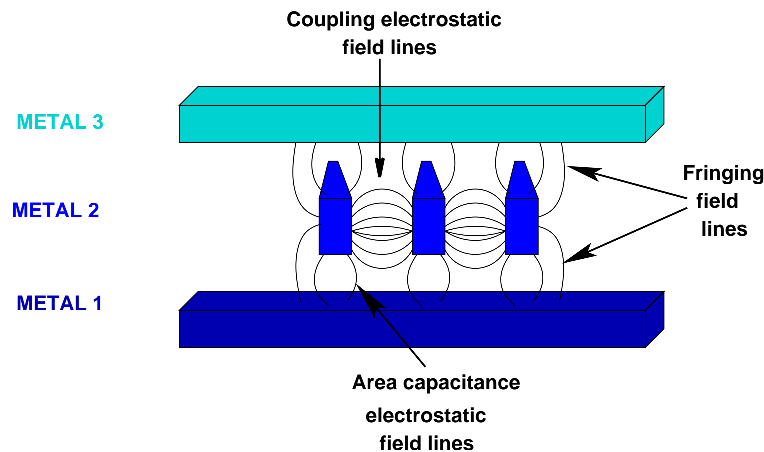

Figure 2.2: The coupling capacitance between interconnects dominates the total interconnect capacitance.

sistivity in order to reduce the RC delay. Decreasing interconnect resistance is achieved using thicker, wider interconnects and also new materials. However, if the resistance of the interconnect is reduced, the currents increase and the inductance become an important factor in multi-coupled interconnects. In Buses with multi-coupled interconnects and long clock distributions, the inductance effects are evident and play an important role in the signal integrity quality [56] [23] [58] [59]. Many techniques have been developed in recent years in order to reduce inductive parasitic effects in high speed interconnects [43] [37] [36] [38].

Low frequency circuits could be modeled like resistive and capacitive devices, and the connection between two of them should be considered as a single node. This approach is no longer applicable in today's high performance circuits, where a good prediction of the behavior is required. High frequency operation at the limit of VLSI circuits cause interconnects to have greater impact on the overall system behavior. Because of the increment in frequency operation and circuit complexity, the wires should be modeled as distributed resistance, capacitance and inductance [56] [5].

Signal integrity is an important factor when determining the reliability and performance of electronic circuits, and many resources are therefore required

to obtain specific signal integrity levels [60] [19] [61] [62] [63]. Signal current variations in a transmission line generate a variable magnetic field. This flux creates induced voltage noise in nearby loops. Shielding techniques have been developed to reduce the mutual inductance of signal lines. This allows induced noise to be decreased [36]. The connections of shielding lines to ground may present resistive open defects [38]. A resistive open appears when the conductive material is not completely broken. Via-contacts are a likely place for opens to occur [64] [65] [66] [67] [68]. Random particle induced-contact defects are the main test target in production testing [67]. In copper-based technologies more defective connections are expected. The number of open defects is greater in copper than in aluminum [69]. These defects indirectly affect the integrity of signal traveling in adjacent signal lines. Ringing values of the signal may vary significantly. Hence, a faulty behavior of the system can occur.

In this chapter, we study the effect of resistive open defects in the grounded shielding line connection. We compare the dominant pole loci of the lumped RLC circuit with distributed RLC circuits in order to determine the region of signal integrity violation. Graphs of overshoot and undershoot values are shown for different interconnect lengths and resistive open defect values.

2.2 Simple interconnect models

The simplest equivalent circuit of a transmission line is a lumped RLC circuit which has a second order transfer function. Varying the inductance from zero to high values, we can plot the trajectory of the equation's roots and identify the over-damping, critical-damping, and under-damping regions. Proper modeling of parasitic interconnect components is required to evaluate the performance of high speed circuits [70] [71]. In [72], the authors model conductors using surface-only triangular meshes. Interactions between Rao-Wilton-Glisson basis functions are used to form a coupled matrix which also includes the modified nodal analysis (MNA) of circuits. This method for modeling interconnects is relatively complex. Furthermore, the use of ideal voltage sources neglects driver impedances and load. A method that generates a passive low order model from a large PEEC(Partial Element Equivalent Circuit)-like circuit models is presented in [60]. In [73] Chen ***et. al*** present a grid model to represent on-chip power bus structures. The meth-

ods mentioned above are complex and require large computation resources to predict interconnect behavior. Interconnects should be modeled in a number of ways, varying accuracy and computational overhead. Problems such as timing, power, noise and reliability can be included in the interconnect model [30].

In this work, we analyze interconnect representation including driver impedance and its equivalent load. The loci of the dominant poles for the equivalent circuit have been used to predict signal integrity violations in the presence of defects.

2.2.1 One stage model

A transmission line can be modeled with a simple equivalent RLC circuit (Fig. 2.3).

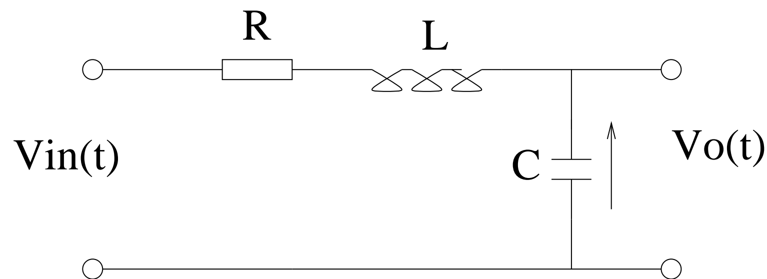

Figure 2.3: Lumped RLC circuit of the interconnect

The characteristic equation considering the driver, line and load is :

$$L(C_i + C_L)\frac{d^2V_o(t)}{dt^2} + (R_i + R_{eq})C\frac{dV_o(t)}{dt} + V_o(t) = V_i(t) \tag{2.1}$$

and
$R = R_i + R_{eq}$
$C = C_i + C_L$

Where $V_o(t)$ is the voltage developed at the capacitance C. R_i and C_i are the interconnect resistance and capacitance respectively, R_{eq} and C_L are the

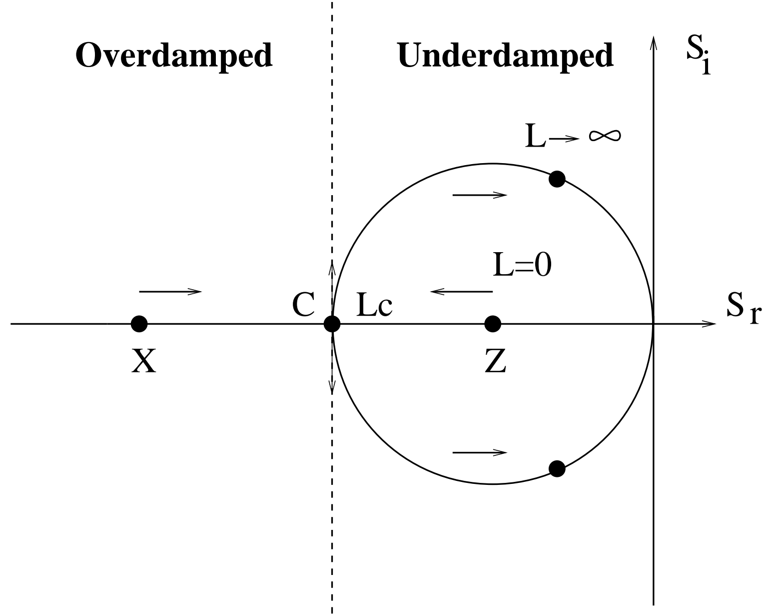

Figure 2.4: Loci of poles of the lumped RLC model of the transmission line as inductance (L) increases

resistance of the interconnect driver and the input capacitance of the load buffer.

Applying the Laplace transform to equation 2.1

$$V_o(s)LCs^2 + V_o(s)RCs + V_o(s) = V_i(s). \tag{2.2}$$

The poles of the transfer function are the solutions of the characteristic equation [5] :.

$$s = \frac{-(RC) \pm \sqrt{(RC)^2 - 4(LC)}}{2LC} \tag{2.3}$$

The track of s on a complex frequency plane when L is increased from a small value to larger values is shown in Fig 2.4. The trajectories start at X and Z for small L, and go through the critical damping point C at $L = L_c$. The critical damping point is obtained when $L = \frac{R^2C}{4} = L_c$. Here s is a pair of complex conjugate numbers in the under-damping region if $L > L_c$. At the point C and for $L > L_c$, the signals present ringings.

2.2.2 Two stage model

A more accurate model of the interconnection is obtained with a two-stage RLC model, as indicated in Fig. 2.5.

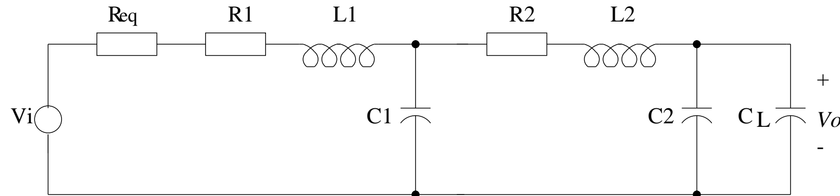

Figure 2.5: Distributed two stage RLC circuit model for the transmission line

The characteristic equation of this system is given by [5]:

$$A4s^4 + A3s^3 + A2s^2 + A1s + 1 = 0 \tag{2.4}$$

where:
$A4 = (L1C1)(L2(C2 + C_L))$
$A3 = (L1C1)(R2C2) + (L2(C2 + C_L))((R_{eq} + R1)C1)$
$A2 = (L1C1)+(L1(C2+C_L))+(L2(C2+C_L))+(R2(C2+C_L))((R_{eq}+R1)C1)$
$A1 = ((R_{eq} + R1)C1) + ((R_{eq} + R1)(C2 + C_L)) + (R2(C2 + C_L))$

The trajectory of the poles of Eq.(2.4) is shown in Fig. 2.6.

Fig. 2.6 shows that two trajectories appear in this case (track 1 and 2). The trajectory with the dominant poles (track1) is the trajectory with the smallest real and imaginary parts.

2.2.3 Three stage model

A model with three RLC stages corresponds to a sixth order system. It has three trajectories of roots where one pole trajectory is also dominant (track1), as Fig. 2.7 shows. If we have distributed transmission line models with more stages, for example four or five, the grade of the characteristic equation grows by a factor of 2*N, where N is the number of stages employed to model the lumped circuit. Thus, we have four roots for a two-stage model, six roots for a three-stage model and so on. In all cases only one trajectory of dominant

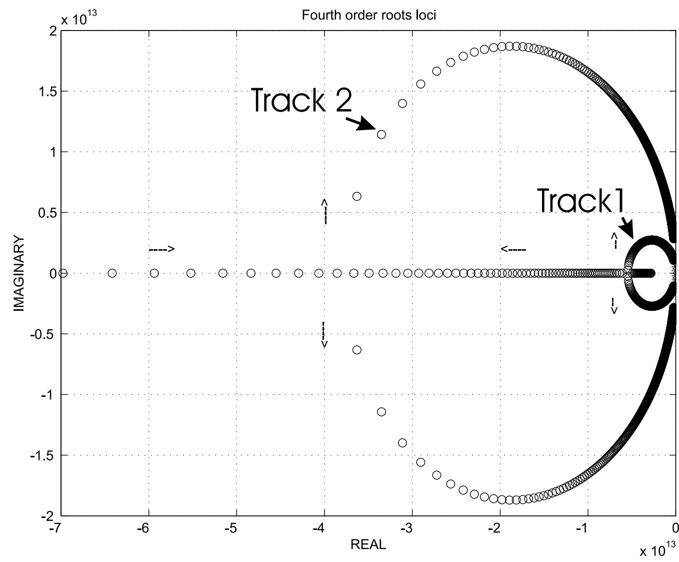

Figure 2.6: Loci of poles of the two-stage distributed model as inductance (L) increases

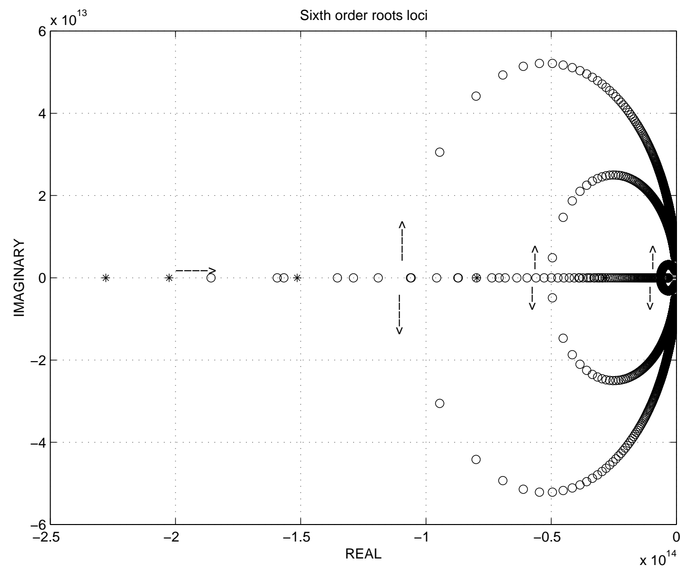

Figure 2.7: Loci of poles of the three-stage distributive model as inductance (L) increases

poles exists, which has roots closer to the imaginary axis and lower frequency oscillation than the other trajectories. Hence, using the dominant poles is a good approximation of the pole trajectories of the second order system. Next, the second order system equation is analyzed in order to obtain an expression for overshoots and undershoots.
The equation of a second order system in the frequency domain is [39]:

$$Y(s) = \frac{w_n^2}{s(s^2 + 2\zeta w_n s + w_n^2)} \tag{2.5}$$

Where w_n is natural frequency of the system and ζ is the damping factor. Applying a unit-step input function and taking the inverse Laplace transform of the equation of the result is:

$$y(t) = 1 - \frac{e^{\zeta w_n t}}{\sqrt{1-\zeta^2}} \sin\left(w_n\sqrt{1-\zeta^2}t + cos^{-1}\zeta\right) \quad t \geq 0 \tag{2.6}$$

The maximum overshoot can be obtained by taking the derivative of Eq. 2.6 with respect to t and setting the result equal to zero. Applying this, we obtain

$$t = \frac{n\pi}{w_n\sqrt{1-\zeta^2}} \tag{2.7}$$

t indicates the time when the ringings of the signal have the maximum a minimum values. The overshoots occur at odd values of n, that is, n=1,3,5,... and the undershoots occur at even values of n. Fig. 2.8 plots $y(t)$ for a $\zeta = 0.2$. It can be observed that the maxima and minima occur at periodic intervals.
The maximum overshoot and the minimum undershoot are obtained substituting eq. 2.7 into eq. 2.6 and setting n=1 and n=2, respectively.

$$maximum\ \ overshoot = y_{max} - 1 = e^{-\pi\zeta/\sqrt{1-\zeta^2}} \tag{2.8}$$

$$minimum\ \ undershoot = 1 - y_{min} = e^{-2\pi\zeta/\sqrt{1-\zeta^2}} \tag{2.9}$$

The poles with the same ζ are located in straight lines on the s-plane passing through the origin and with slope $\pm\frac{\sqrt{1-\zeta^2}}{\zeta}$. ζ is correlated with the interconnect parameters as $\zeta = \sqrt{\frac{R^2C}{4L}}$. Where R, L, and C are the resistance, inductance, and capacitance related with the interconnect respectively.

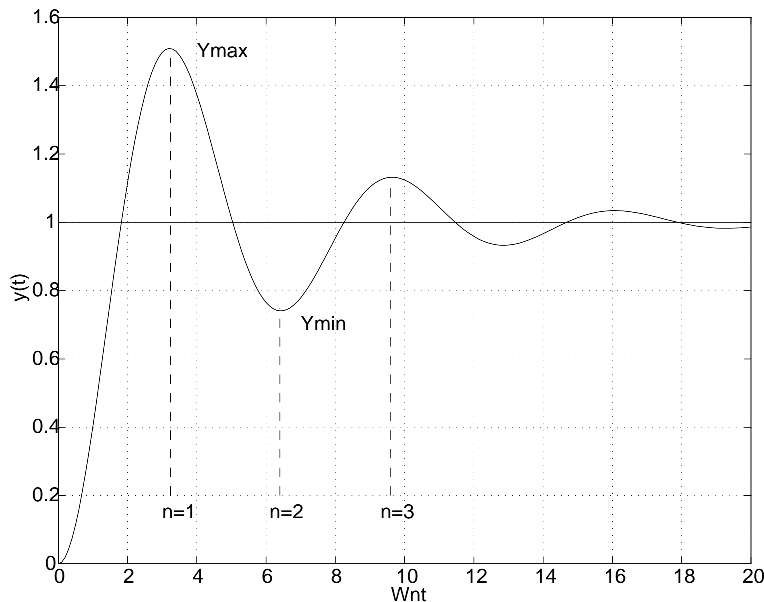

Figure 2.8: Transient response for the Second order system for a unit step signal. Maxima and minima of the response are indicated (n=1,2,3)

The dominant poles located in the lines have the same ζ and consequently the same overshoot (undershoot). Later these lines will be used to determine the signal integrity regions on the s-plane (see Fig. 2.17). Table 2.1 shows pole values for the lumped and the distributed models of interconnects. Hspice internal field-solver tool has been used in order to obtain the interconnect parameters. Using the extracted parameters, electrical simulation were made to obtain the dominant poles. In our case, the dominant poles have the minimum real and imaginary values. Hence, if only a pair of poles has important information, they correspond to a Second order system. The values of the overshoot and undershoot can be estimated with this approximation.

2.3 Shielding practice

Shielding lines are used to reduce the coupling inductance effect of a transmission line [15] [36] [74]. Shielding lines are grounded to the substrate, and

Model	Simulation Pole Value	ζ
lumped	-1.1446E+10±2.3441E+10i	0.438
dist2	-1.2449E+10±2.7623E+10i	0.41
dist3	-1.2525E+10±2.9212E+10i	0.394
dist4	-1.2725E+10±3.0035E+10i	0.390
hspice	-1.3329E+10±3.3137E+10i	0.373

Table 2.1: Pole values for 1, 2, 3, 4, and 20 stage model having dominant poles in all cases

placed between signal lines in order to reduce mutual inductance between signal lines. When the shielding lines are inserted between two critical lines, almost all capacitive coupling noise between the two lines are eliminated. The shielding lines also help to reduce the self-inductance effects of a line by generating a current return path very close to the signal line [75] [76]. This also reduce the inductive coupling between lines of either side of the shield. Several kind of conductive shielding lines could be implemented like shields connected to VDD or GND or active shields [37] [77] [78]. In this work, the case of the shield connected to GND is analyzed. Fig 2.9 shows the interconnect system structure used for simulation analysis. The dimensions H, S, W and T represent the height, separation, width and thickness of the interconnect, respectively. Each signal line is located between two shielding lines

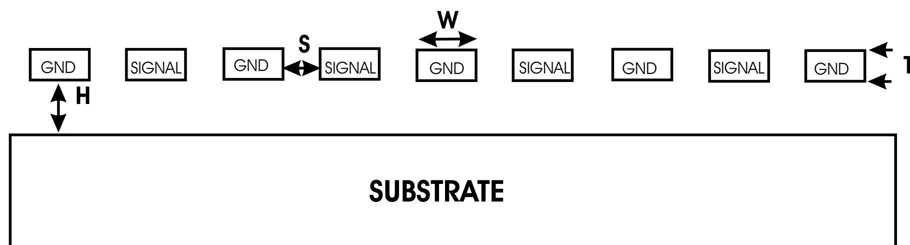

Figure 2.9: Bus system with shielding lines

in order to reduce crosstalk noise. This shielding technique has high area overhead. However, it is widely used for high speed signal systems with long interconnects [36] [34].

Shielding lines are grounded to the substrate at each end of the line. Open defects in one ground connection in the shielding line may produce a degra-

dation of the shielding function. Fig. 2.10 and 2.11 show the faulty-free shielding line connection and faulty shielding line connection, respectively. If an open exists, it could be modeled as resistive open (Fig 2.11) with

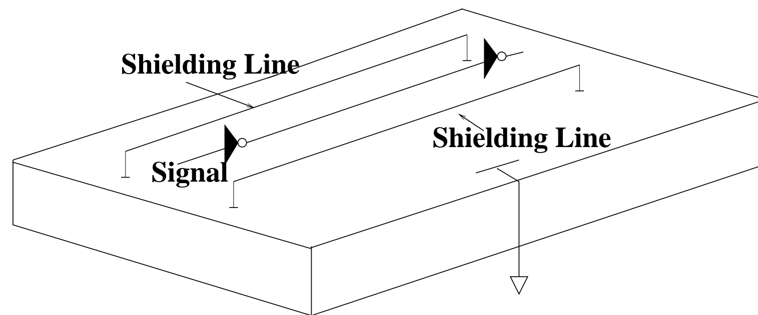

Figure 2.10: Grounding the shielding line at both ends of the shield.

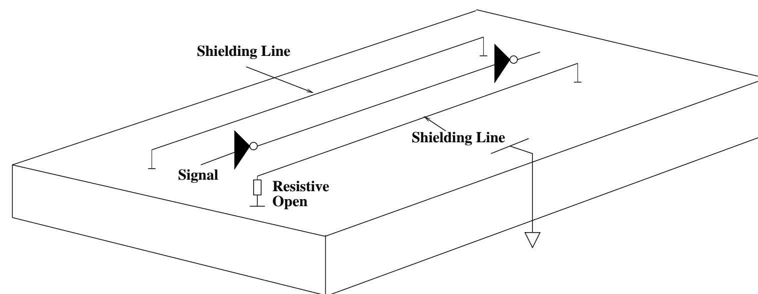

Figure 2.11: Faulty shielding due to a resistive open in the grounding connection.

different resistance values. Realistic resistive opens have values from some tens of ohms to some hundred kilo ohms[64]. In this experiment we take into account resistive opens from 100Ω to 150 $K\Omega$. Above 150 $K\Omega$ (even for full open defects) the behavior is similar to 150 $K\Omega$. Fig. 2.12 shows the case for a resistive open in one ground connection.

In the next section we analyze the signal integrity of signal behavior when a defect (resistive open) occurs in the shield ground connection.

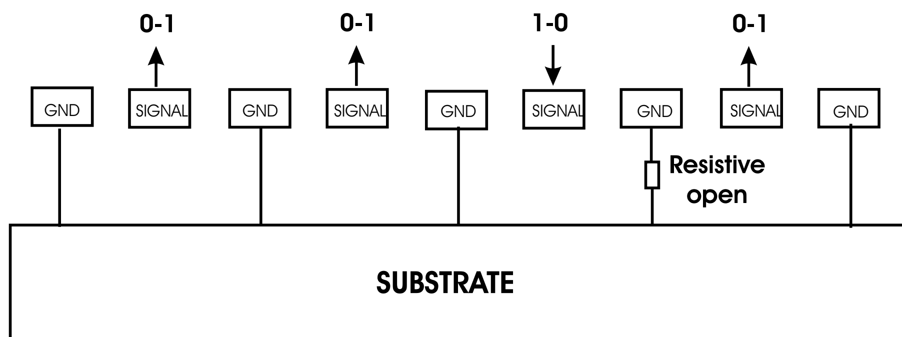

Figure 2.12: Faulty ground connection in one shielding line having a resistive open with the worst case excitations.

2.4 Characterization of signal quality

In general, integrity of a signal indicates its compliance of the static and dynamic logic signal specification [46] [79] [80]. In practice, logic circuits can tolerate some levels of noise. For example, a CMOS gate interprets as logic 1 input voltages in the [V_{H_imin}, V_{DD}] range and any voltages in the [V_{ss},V_{L_imax}] range as a logic 0 (See Fig 2.13). Electronic circuits allow some amount of delay skew i.e. $T-SI-R$ and $T-SI-F$ for rising and falling delays. In this work the minimum undershoot and the maximum overshoot (Fig 2.13) on shielded bus lines are investigated. Undershoots and overshoots that are outside of the immune region produce a signal integrity violation. For example, a signal integrity violation occurs if the overshoot is bigger than V_{L_imax} voltage level as indicated by 2.10:

$$\frac{Overshoot}{V_{L_imax}} > 1 \tag{2.10}$$

We have considered four signal lines switching simultaneously, one of them in the other direction of the others (See Fig. 2.12). Each one is located between two shielding lines. One of the shielding lines has a resistive open defect in one side. The effect on the signal traveling next to the defective shielding line is studied. Resistive opens with values of 100 200, 300, 500, 1K, 10K, 100k and 150K ohms are used for interconnect lengths of 1, 2, 3, 4, and 5 mm and three different drivers. The aspect ratio of the nominal driver is modified ±50%. We use 100nm MOS technology for Hspice simulation with a $V_{tn} = 260mV$, $V_{tp} = -303mV$ and $V_{DD} = 2.5$ [81].

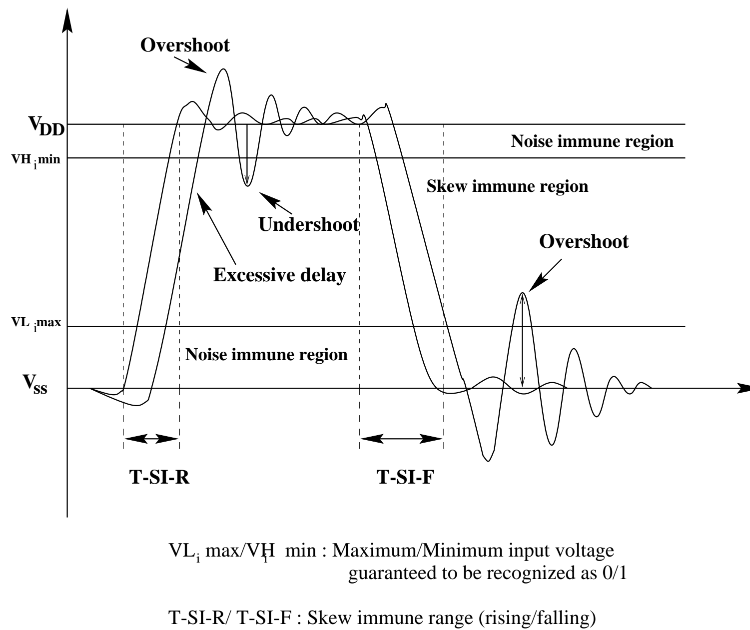

Figure 2.13: Integrity loss due to undershoot and overshoot in long interconnect lines.

Fig 2.14 shows the overshoot versus interconnect length using the nominal driver. The value of overshoot is normalized to Vtn. For lines below 2.3mm and resistive opens above 300Ω may show signal integrity violation (SIV) with $\frac{Overshoot}{V_{L_i max}} > 1$. Resistive opens of $1K\Omega$ could produce SIV in lines

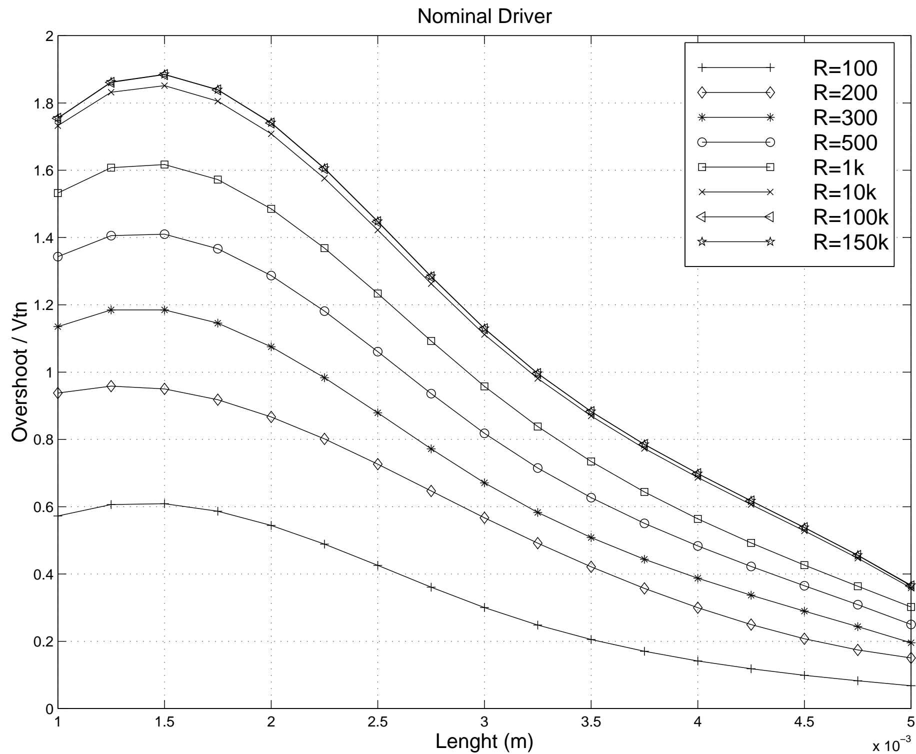

Figure 2.14: Overshoot Vs Length of the interconnect with a defective (resistive open) shield. R values from 200Ω to 150 $k\Omega$ and Length values from 1mm to 5mm with a nominal driver

shorter than 2.9mm. For full open ($R = \infty$) defects on the shield the SIV may appear in lines shorter than 3.3mm. Increasing 50% the size (channel width) of the nominal driver, the SIV in lines shorter than 3.6mm become visible for resistive opens with 100Ω (See Fig. 2.15). Resistive opens above 300Ω may cause SIV for lines below 5mm. Fig. 2.16 shows the overshoot versus interconnect length where the nominal driver is decreased 50% in size. In this case, a resistive open defect on the shield of 300Ω produces SIV in lines below 3.3mm. Lines shorter than 4.6mm may have signal integrity problems if a resistive open defect on the shield occurs with values above $1k\Omega$.

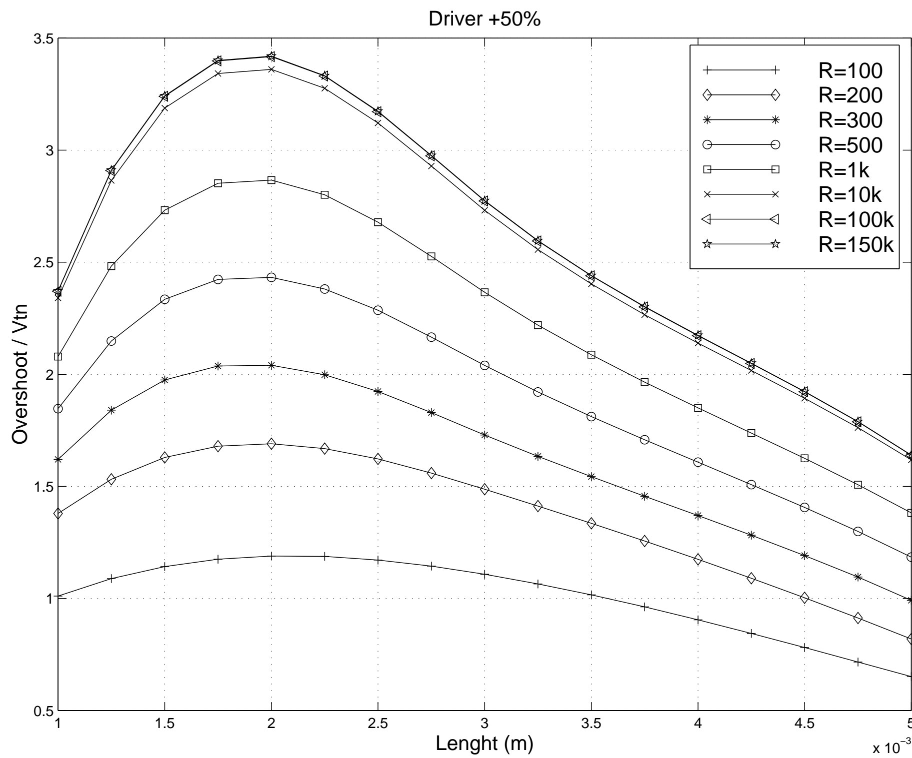

Figure 2.15: Overshoot Vs Length of the interconnect with a defective (resistive open) shield. R values from 200Ω to 150 $k\Omega$ and Length values from 1mm to 5mm with 50% higher driver than nominal driver.

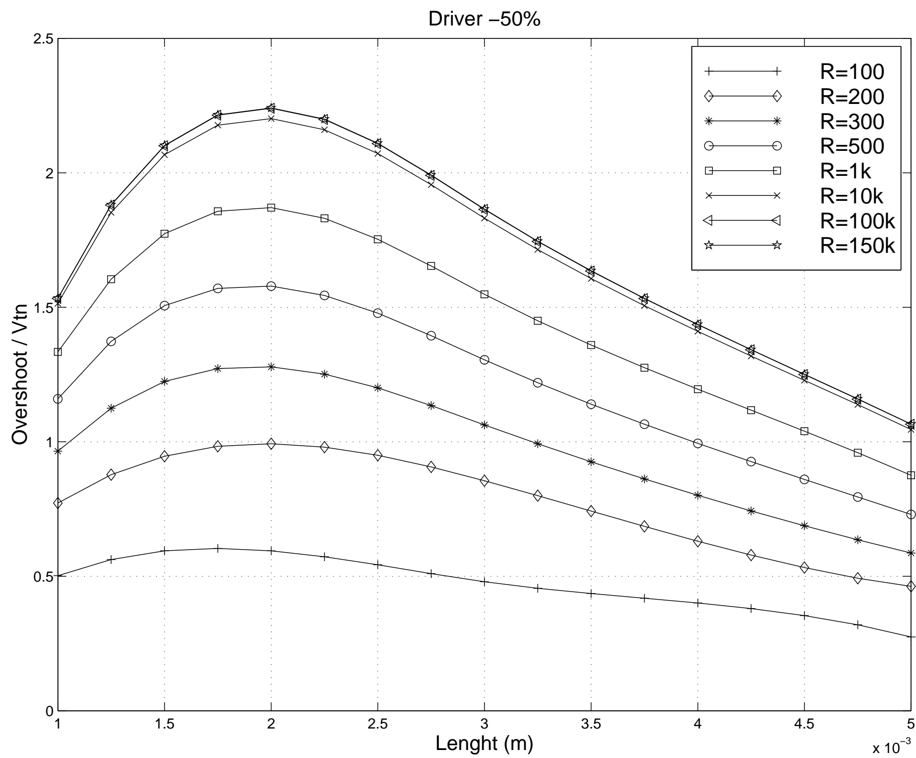

Figure 2.16: Overshoot Vs Length of the interconnect with a defective (resistive open) shield. R values from 200Ω to 150 $k\Omega$ and Length values from 1mm to 5mm with a 50% smaller driver than nominal driver.

2.5 S-Plane signal integrity regions

As shown in the previous study using electrical simulations, a defective shield connection may change the signal integrity quality. Resistive open defects of a shielding line affect the shielding function. Because of this, the characteristics (RLC) of the signal lines next to it are modified. The dominant poles can be plotted in order to establish its loci in the S-plane. The poles in Figs. 2.17, 2.18, and 2.19 are the dominant poles, they were extracted from the output waveform obtained by Hspice simulation on the bus system showed in Fig. 2.12. The three different aspect ratios of the driver are used. The two areas for acceptable and non-acceptable signal integrity regions are indicated in Fig. 2.17 for a nominal driver. Figs. 2.18 and 2.19 show the same areas, but with a decreased and increased driver size, respectively. Pole loci allows to determine if the resistive open produce or not a signal integrity violation. For a resistive open value of 300Ω, the level of ringing become higher than V_{tn} using the nominal driver and the decreased driver size. If the increased driver sized is used, the ringing could be higher than V_{tn} for resistive open defects above 100Ω. Increasing the value of the resistive open results in a change of the waveform shape. Hence, there is a change in the pole loci as Figs. 2.17, 2.18, and 2.19 show.

2.6 Conclusions

The signal integrity in shielded transmission bus lines has been studied and characterized by electrical simulation. Shielding lines help to decrease inductance and capacitance coupling in long interconnects. These lines are grounded to the substrate by vias. If a resistive open occurs in this ground connection the impact on signal interconnects may produce signal integrity violations. It has been found that in presence of resistive open defects on shielding lines, the neighboring signals could fall out of the noise immune regions. Hence, this may produce a faulty behavior of the next gate or block that is driven by the affected interconnect.

The trajectory of the roots of the characteristic equation shows the interconnects behavior when the inductance varies. The inductance changes with interconnect geometry. For thicker and wider interconnects, the resistance per unit length is reduced significantly, hence the inductance effects become

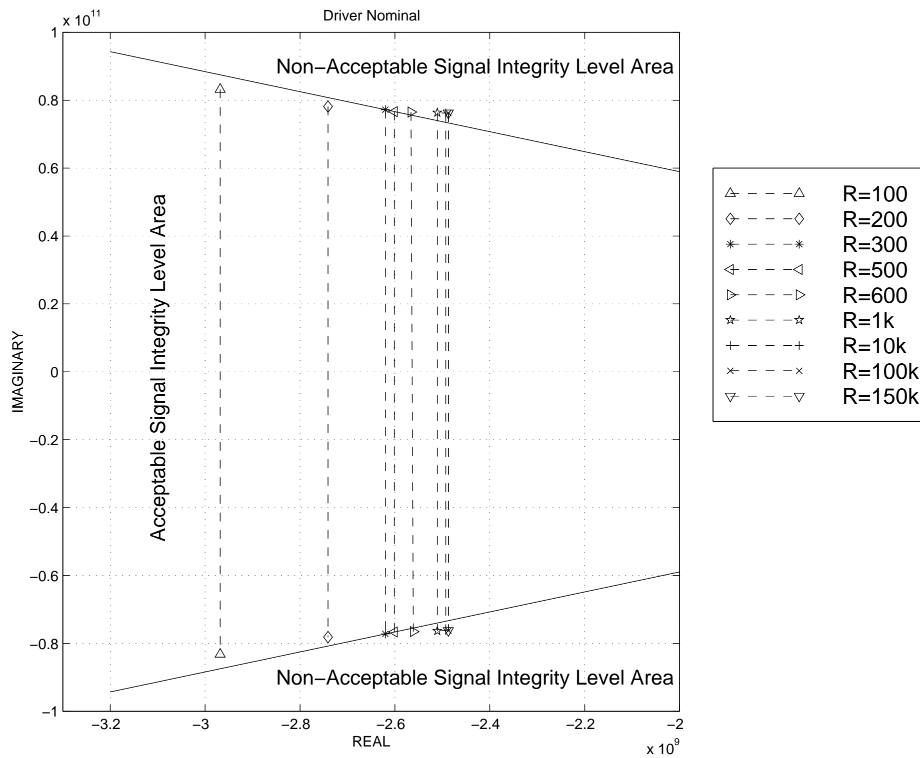

Figure 2.17: Pole loci for different resistive opens on the shield for a bus interconnect of length l=2mm and using nominal driver.

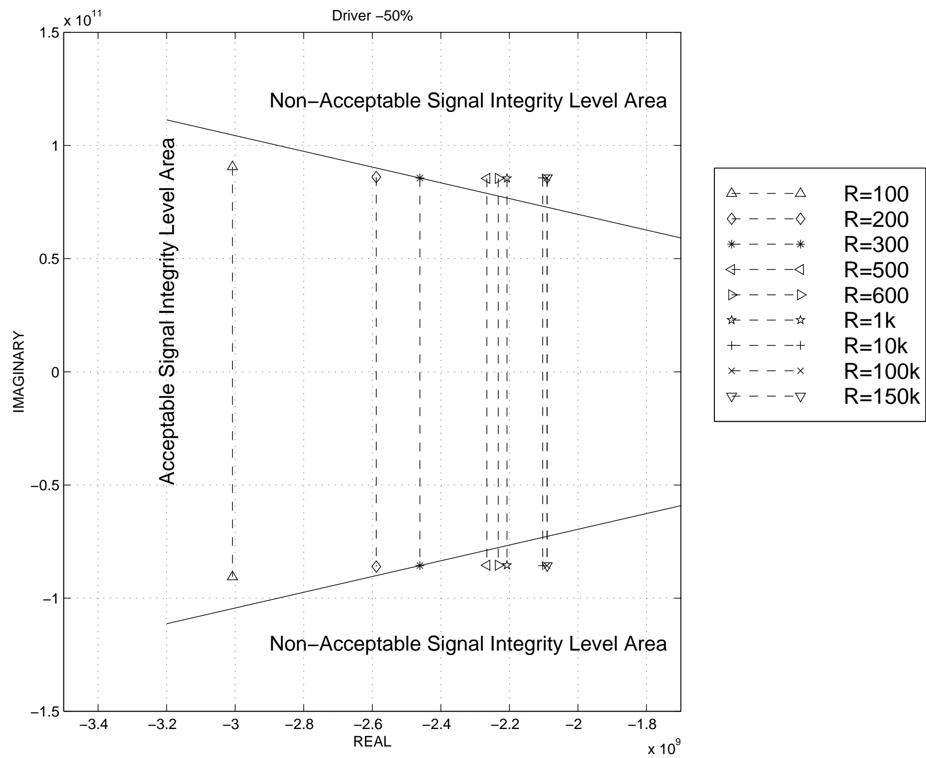

Figure 2.18: Pole loci for different resistive open on the shield for a bus interconnect of length l=2mm and using decreased driver.

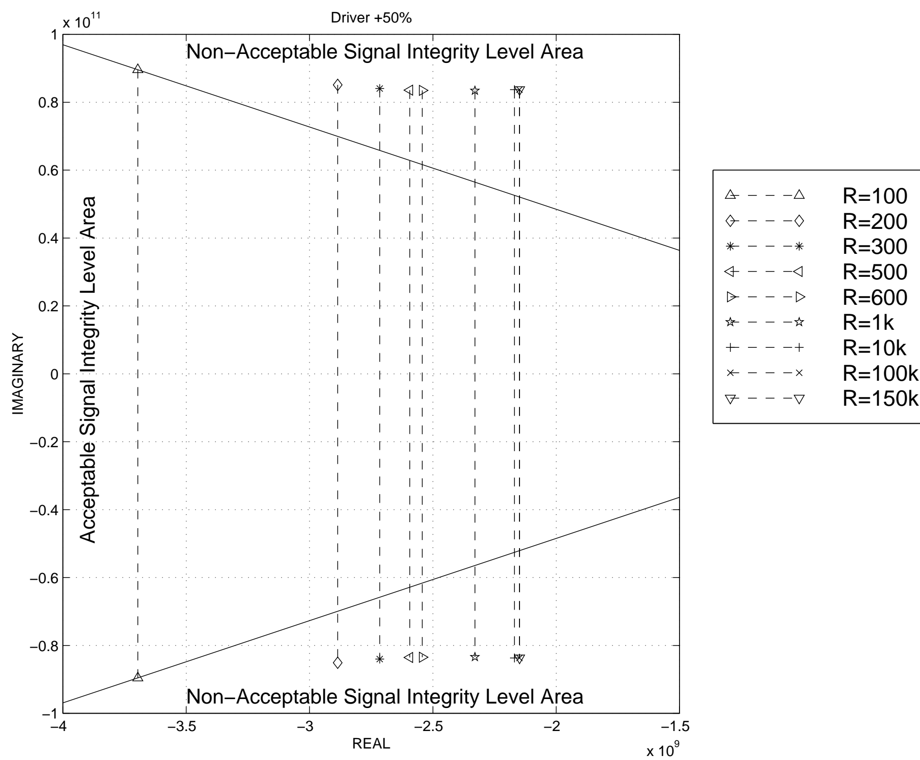

Figure 2.19: Pole loci for different resistive open on the shield for a bus interconnect of length l=2mm and using increased driver.

important. Also, using new low resistive metals helps to increase the inductance effects.

The property of the trajectory roots can be used to identify if the interconnect has an underdamping or overdamping deportment. It is shown that for an N-stage model we have N trajectories for the poles but only one is dominant. Thus a pair of dominant poles is sufficient for signal integrity analysis. The signal integrity level taken in this work was established for 100nm technological parameters and the measurement values of overshoots was normalized with respect to V_{th_n}.

Acceptable and non-acceptable signal integrity regions were established with the pole loci. A line placed from 0 and crossing the first complex pair of pole that cause signal integrity violation helps to determine the area for signal integrity violations. The overshoot is analyzed for different resistive open values in the grounded shield connection and for three different sizes of driver. It is shown that for resistive opens with $1K\Omega$ and using nominal driver could produce SIV in shorter lines than 2.9mm. For full open $(R = \infty)$ defects on the shield the SIV may appear in shorter bus lines than 3.3mm. Increasing by 50% the size of the nominal driver affects the transmission line behavior. The SIV in lines below 3.6mm become visible for resistive open defects with 100Ω. Resistive open defects with values above 300Ω may cause SIV for lines below 5mm. When the nominal driver is decreased 50% in size, resistive open defect on the shield with 300Ω could cause SIV in lines below 3.3mm. Shorter lines than 4.6mm may have signal integrity problems if a resistive open defect on the shield occurs with values above $1k\Omega$. The size of the driver, together with resistive open defects, have an important impact on pole loci. Hence, the behavior of the transmission line is changed.

Chapter 3

Verification of signal integrity using High Speed Monitors

Signal integrity verification is becoming an important issue as technological process features continues to shrink and logic speed increases. Advanced technologies permit to integrate a large number of devices onto a chip. Current high performance systems require to assure good levels of signal integrity. In this chapter a signal integrity verification methodology is presented. The chapter presents an introduction of the signal integrity as a problem in current high performance integrated circuits. Next a methodology to verify the signal integrity is proposed. Sensors to monitor the signal integrity are proposed. The resulting cost for implementing this signal integrity methodology is evaluated. Next, the sampling technique used in this proposal is described. The strategy to generate the control and enable signals for the monitors and the possible measurement errors of the proposed methodology, are also explained in this chapter.

The rest of the chapter is organized as follows: In section 3.1 an introduction for signal integrity issues in current technologies is presented. A methodology for signal integrity verification is proposed in section 3.2. Next, the proposed sensors to monitor the signal integrity violation are presented in section 3.3. Section 3.4 presents the coherent sampling technique used for the proposed methodology. The monitoring system architecture is presented in section 3.5. In section 3.6 and 3.7 the accuracy and cost of the proposed methodology is evaluated. Finally the conclusions of the chapter are given in section 3.8.

3.1 Introduction

While nanometric technologies enable to integrate circuits (ICs) with more functionality, transistors per μm^2, interconnect density, etc. [14] [82] [83], the designer needs to prevent problems as crosstalk noise, substrate noise, power supply voltage drop, etc. [9] [5] [57] [8]. All these factors can affect the SI and may produce an unreliable performance of the system. Preserving signal integrity (SI) in complex designs is a current challenge in nanometric technologies [20] [84] [85].

Signal integrity could be defined as the ability of a signal to generate assured correct responses in a circuit. *A signal with good SI has digital levels with required voltages levels at required times* [7]. For designers good levels of SI means clean data, free of ringings, and not sensitive to interferences. However, high performance systems, for example SoCs (Fig. 3.1), made in nanometric technologies, lead to have signals with unavoidable noise levels. Digital and analog cores can share the same substrate, the noise generated by the digital core could affect the performance of analog core.The large amount of interconnects in current integrated circuits, carrying out high speed signals, interact between them by the action of parasitic elements producing signal integrity degradation [86] [87] [88].

Digital and mixed-signal circuits can be affected by internal switching noise [89] [90]. Internal noise, for example interference noise, is caused by internal transient currents flowing through the package parasitics. These currents are generated by the synchronized switching activity of the millions of the digital gates of the chip. These injected currents, substrate noise and voltage fluctuations of the power/ground lines could affect the performance of the digital and sensitive analog/mixed signal circuits [91] [92] [93]. Other source of internal noise is the electromagnetic environment in which the electronic systems have to work. The electromagnetic phenomenon is caused by the high rates of the switching activity of the signals traveling on the interconnects [94]. External noise could be generated by the radiation of the chip to chip interconnects that behaves like antennas. Current spikes generated by the high speed signals can affect the performance of the components mounted on the same board [14] [22] [95]. In general, integrity of a signal indicates its compliance of the static and dynamic logic signal specification [96] [46].

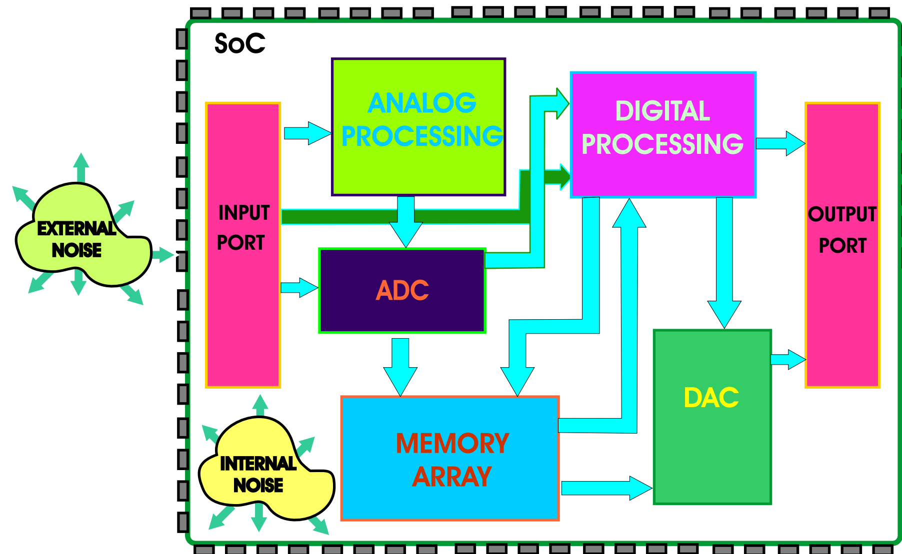

Figure 3.1: SoC structure example: Several analog and digital blocks work together

In practice, logic circuits can tolerate some noise levels. For example, a CMOS gate interprets as logic 1 or 0 if the input voltages are inside of the permitted noise margin region as Fig. 3.2 shows [46]. However, voltage levels in the middle region (see Fig. 3.2) may not be interpreted correctly by the next stage.

The voltage magnitude (NH) and the duration (NW) of the noise pulse over the signal determine the performance of the circuit receiving that noisy signal. NH is the voltage quantity that a high (low) logic level drops (rise) from VDD (GND). NW is the duration time of the noise pulse.

In the next section the proposed signal integrity verification methodology is presented.

3.2 Proposed Verification Methodology

Signal Integrity violation (SIV) occurs when the signal digital levels do not have the required voltages to achieve the correct performance. Signal ringings with forbidden voltage values are examples of SIV. Detecting (SIV) and

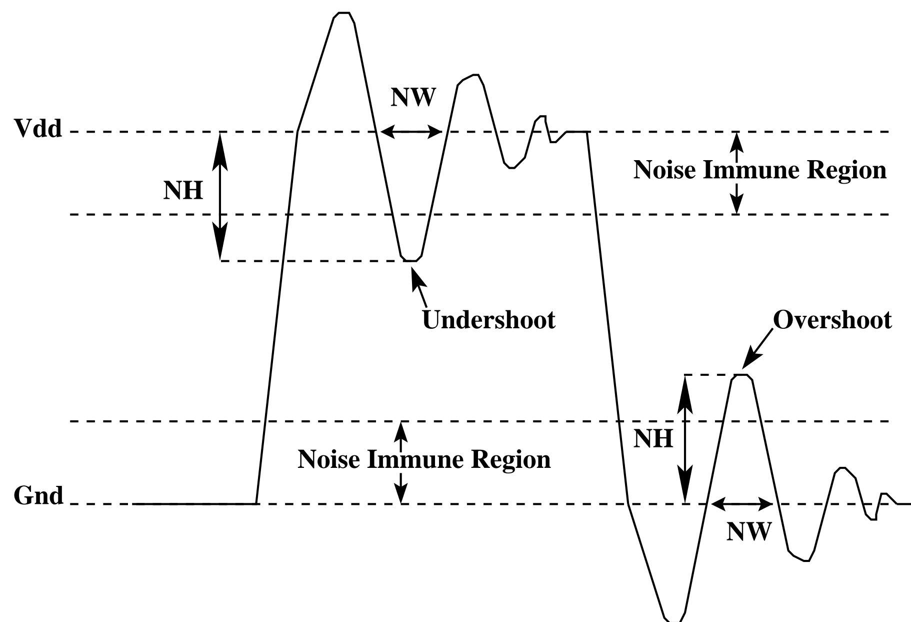

Figure 3.2: Signal having undershoot and overshoot outside of noise immune region. NH and NW are the voltage noise magnitude and the noise width respectively.

evaluating the obtained results by the monitors require an efficient methodology to ensure that all SIVs are being captured and processed without loss of information. Assuming that proper periodic input signals are applied to the block A (See Fig. 3.3), the signals arriving to the block B have a periodical behavior and some, or all of them, could be under verification. The block A could be any circuitry that generates periodic signals and the block B could be any circuitry that receives the signals generated by block A. These blocks are connected by on-chip metal lines. In this block diagram the block A and B are connected by long metal lines (interconnects in the range of millimeters) which may be affected by several sources of noise (capacitive and inductive coupling, reflections, radiations, etc.) .

Two monitors (sensors in Fig. 3.3) are required for detecting the SIV, one of them is for monitoring SIVs at the high level (undershoots) and the other one is for monitoring SIVs at the low level (overshoots). The monitors are physically placed near to the block B or in a general way, near to the point where the sample of the signal under verification (SUV) is taken. Each monitor receives three signals at the time of test: a) the first one is the SUV from a point near to the block B, b) the second one is the sampling signal which has a coherent frequency [97] [98], and c) the third one is an enable signal. The coherent sampling generator block receives at its input the system master clock and by internal circuitry the clock signal is processed in order to obtain the required coherent frequency. The sampling signal generated by this block requires special features to obtain the effective sampling frequency for getting the overall information of the SUV [97][99].

The verification methodology uses an undersampling technique, called coherent sampling [97] [100]. Coherent sampling takes samples with high precision with relatively low sampling frequency. This allows to analyze the output of the monitors at low frequency rates and relaxing the design effort of the overall verification blocks. More details about how the coherent sampling frequency is generated will be given later. The enable signal is generated by the "**enable generator**" which takes samples of the SUV at the rate of the sampling frequency. Using both signals the circuitry inside of the block generates the signal **EM**, this signal enable either the high or low level sensor. Also this block generates the enable signal **ER**, where **ER** activates the corresponding registers for storing the output of the high or low level sensors. The monitor output analyzer receives and stores the high and low level

monitor output. This information is sent outside of the chip by an external pin to inspect externally the monitor outputs. Each one of the blocks will be explained later in more detail.

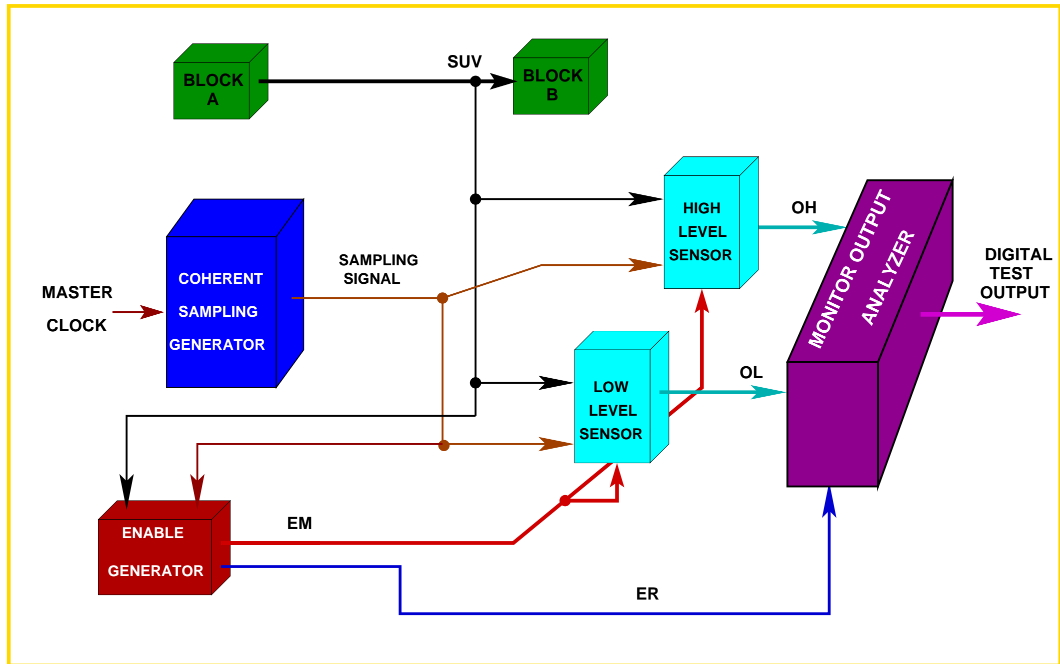

Figure 3.3: Block diagram of the general verification methodology.

3.3 Proposed sensors

Detection of signal integrity violations (SIVs) is the goal of our methodology. To carry out this, monitors able to sense these violations of integrity (undershoots, overshoots) are needed. Two monitors are proposed for sensing SIVs, specifically when undershoots and overshoots occur in a signal (See Fig. 3.2). High level SIV monitor senses integrity violation when a digital signal has ringings in the high logic level. If ringings are below of the threshold voltage of a gate that receives this signal, it could be interpreted erroneously as low logic level. In another hand low level SIV monitor sense integrity violation

when a digital signal has ringings in the low logic level.

Next subsections explain the behavior of the proposed high and low level monitors. High and low level monitors able to verify more than two signals are also presented. In the last subsection monitor performance has been characterized by function of noise width (NW) and noise height (NH).

3.3.1 High level SIV Monitor

High level SIV Monitor consists of a differential pair with a latch as load (See Fig. 3.4). This architecture is similar to that proposed for the Mixed signal monitor [47]. The latch acts as load of the monitor. This latch is built with two cross-coupled PMOS transistors. It helps to switch the nodes X and XN to complementary logic levels. The load on the nodes X and XN and the size of T_{in1} and T_{in2} determine the speed of switching. Precharge transistors $Tp1$ and $Tp2$ must be designed to minimize load at nodes X and XN.

The methodology used to verify the SUV is as follows. The verification is

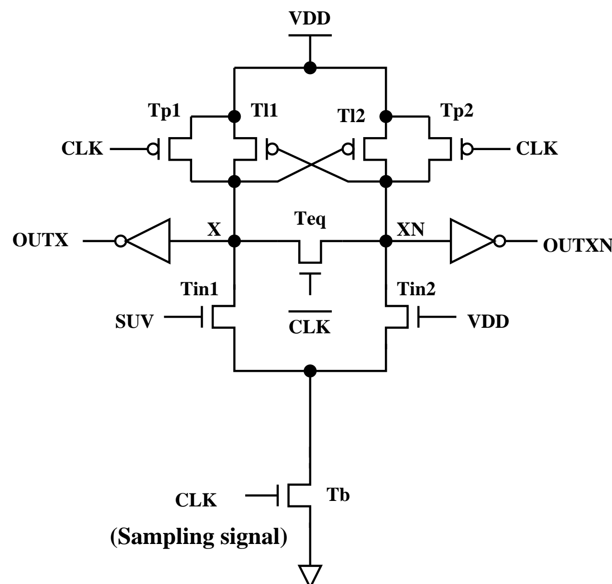

Figure 3.4: High level signal integrity violation monitor.

made in two steps, in the first step a pre-charge operation takes place by

transistors T_{p1} and T_{p2}, when CLK is low, transistor T_{eq} helps to equalize nodes X and XN to V_{DD}. Transistor T_b is off, therefore no current path to GND exists through T_b. In the second step CLK is high and the transistors T_{p1}, T_{p2} and T_{eq} are off. One input transistor (T_{in1}) receives the signal under verification (SUV) and the other one (T_{in2}) has a reference voltage as input that in this case is V_{DD}. The aspect ratio (W/L) of T_{in1} is larger than T_{in2} such that if the SUV is equal to V_{DD} the node X is discharged to GND by T_{in1} and T_b. The different aspect ratios establish a threshold detection voltage of the monitor.

If the SUV has a value below of the threshold detection voltage, the node X remains to V_{DD} while the node XN is discharged to GND therefore a SIV is detected. This switching action is helped by the latch formed by the transistors T_{l1} and T_{l2}. Timing curves showing the behavior of the nodes X and XN are shown in Fig. 3.5. Time $t1$ is the time required for the monitor to have the precharge voltage levels. Time $t2$ is the time required to begin the evaluation of the SUV. Tp is the duration of the precharge stage and it must be longer than $t1$. The time te is the duration of the evaluate stage and it must be longer than $t2$.

3.3.2 Low level SIV Monitor

Low level SIV Monitor is a PMOS-Input differential pair with a latch made with NMOS transistors as Fig. 3.6 shows. The behavior is complementary to the high level SIV monitor. In this case, ringings that occur in a low logic level can be detected by the low level SIV monitor.

When CLK is high the nodes X and XN are discharged to GND by transistors T_{p1}, T_{p2}, transistor T_{eq} equalizes nodes X and XN to GND. The sensing action of the monitor begins when CLK is low. The reference voltage in this case is GND. The aspect ratio between transistor T_{in1} and T_{in2} are different in order to have a threshold detection voltage. If the input signal (SUV) is a 0 logic level or below the threshold detection voltage, the node X will be charged toward V_{DD} by the action of transistors T_b, T_{in1} and those in the latch formed by T_{l1} and T_{l2}. If the input signal is above the threshold voltage detection (an integrity violation) the node XN will be

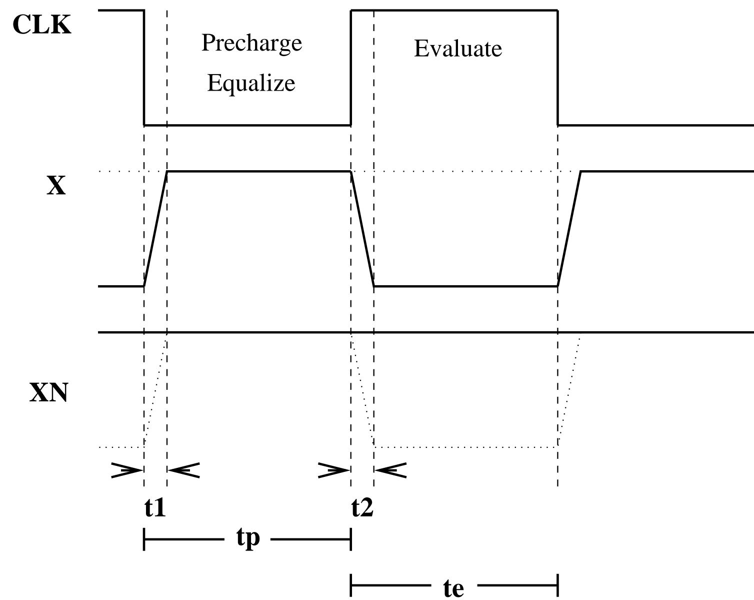

Figure 3.5: Behavior of the signals at nodes X and XN under verification mode. Continuous line no SIV, dotted line SIV.

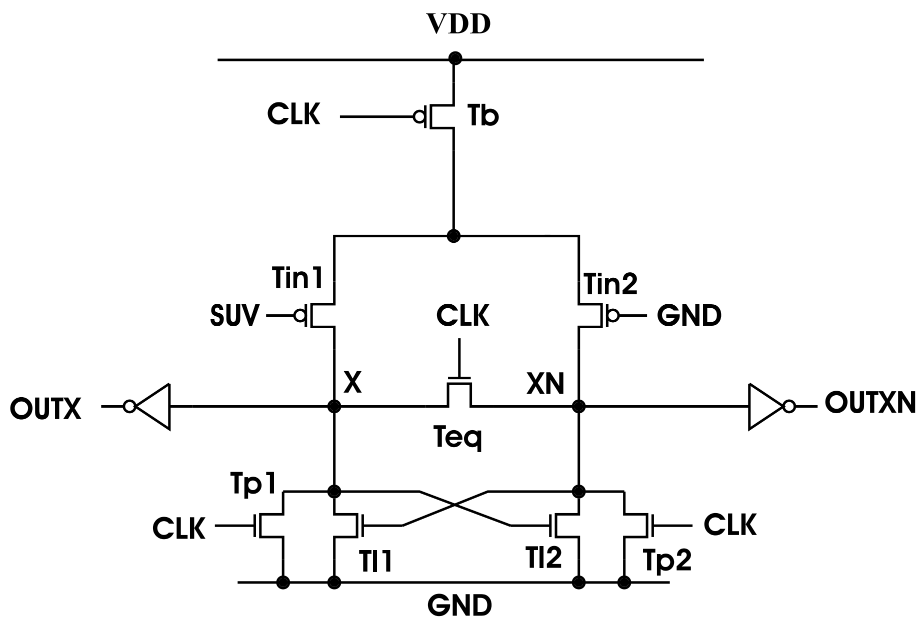

Figure 3.6: Low level signal integrity violation monitor.

charged toward V_{DD} by T_b and T_{in2}. The latch speed-up the switching action.

As explained above, the monitor behavior consists in precharge the nodes X and XN to GND (precharge phase) and evaluating the SUV with a reference voltage (evaluating phase). The ideal behavior of X and XN at these two phases is shown in the timing curves depicted in Fig. 3.7. tp is the time required for the precharging phase and te is the time needed for the evaluating phase.

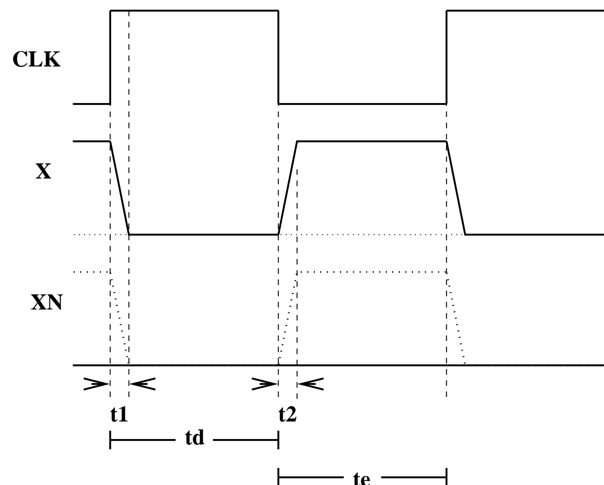

Figure 3.7: X and XN behavior in one CLK period. Continuous line no SIV, dotted line SIV.

3.3.3 Multi-signal Monitors

The monitors mentioned above have been adapted in order to sense multiple signals. The schematic of the modified monitors for the high and low level signal integrity monitors are shown in Figs. 3.8 and 3.9.

Adding equal n number of transistors in both input sides of the monitor (input an reference signals) and pair of enable transistors (signals E_n), where n is the number of signals under verification, is possible to verify several signals. One signal is verified at a time enabling the control signal E_n that corresponds to the signal under verification. Equal number of input transistors and reference transistors are required for having the same load in the

Figure 3.8: High level signal integrity violation monitor with multi-input signals.

nodes X and XN. In a similar way, the low level signal integrity monitor has been modified to sense multiple signals.

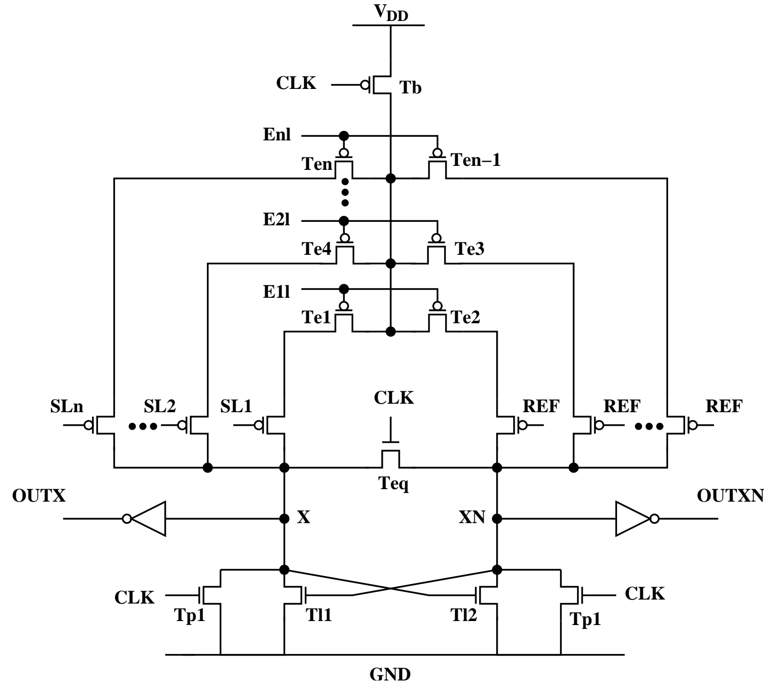

Figure 3.9: Low level signal integrity violation monitor with multi-input signals.

3.3.4 Monitor Performance

The performance of the high (low) level monitor is characterized by the width, NW, and height, NH, of the signal going below (above) V_{DD} (GND) (See Fig. 3.2). Well defined rectangular shapes for the undershoots and overshoots have been considered. It has been considered a monitor with only one input signal to verify. The monitor design effort has been focus on detecting the noise pulse with the minimal duration. Monitor transistor are sized in order to obtain this goal. The transistor channel widths are indicated in Table 3.1. All of the channel length are the minimum allowed by the technology (180nm).

Table 3.1: Widths of the monitor transistors

Transistors	High level monitor (μm)	Low level monitor (μm)
Tl1,Tl2	15	3
Tp1, Tp2	2	3
Teq	10	10
Tin1	5	8
Tin2	3	3
Ten	4	8
Tb	10	15

TSMC 0.18 microns CMOS technology is used to evaluate the monitor performance. Hspice electrical simulations have been made to observe the behavior of monitor outputs when a SUV is analyzed. The high logic state integrity is verified by the high level SIV monitor the output responses of the monitor are shown in Fig. 3.10 and 3.11. Fig. 3.10 shows the case when SIV occurs.The upper panel shows the used SUV. Next panel is the CLK signal. The third panel shows the signal at node $OUTX$, which corresponds to the buffered signal of the voltage at node X. The signal at the node $OUTXN$ is shown in the lower panel. This signal is complementary to signal $OUTX$ only when CLK is high. The cross-coupled PMOS transistors keep these voltage levels at the nodes $OUTX$ and $OUTXN$ while the CLK is high.

When a SIV occurs (Fig. 3.10), the node X remains charged because the noise pulse does not have sufficient energy (voltage and time duration) to be interpreted as a 1 logic. Therefore T_{in1} does not have the enough current capability to discharge the node X generating node $OUTX$ becomes a logic 0. The node XN is discharged by T_{in2}. It is on due to the constant reference voltage (REF) at its gate. The node $OUTXN$ becomes a logic 1 by the action of T_{in2} and the monitor latch.

Fig. 3.11 shows the case when a SIV does not occur. In this case, the voltage level (VDD) in the high logic state of the SUV (upper panel) corre-

spond to the voltage level allowed for logic 1. When CLK become high, the input transistor T_{in1} is on and hence, the node X is discharged by T_{in1} and (T_b). The buffered signal $OUTX$ shows this action in the third (from top to bottom) panel of Fig. 3.11, the complementary signal $OUTXN$ is depicted in the bottom panel.

The detectability regions for the high level monitor are shown in Fig. 3.12.

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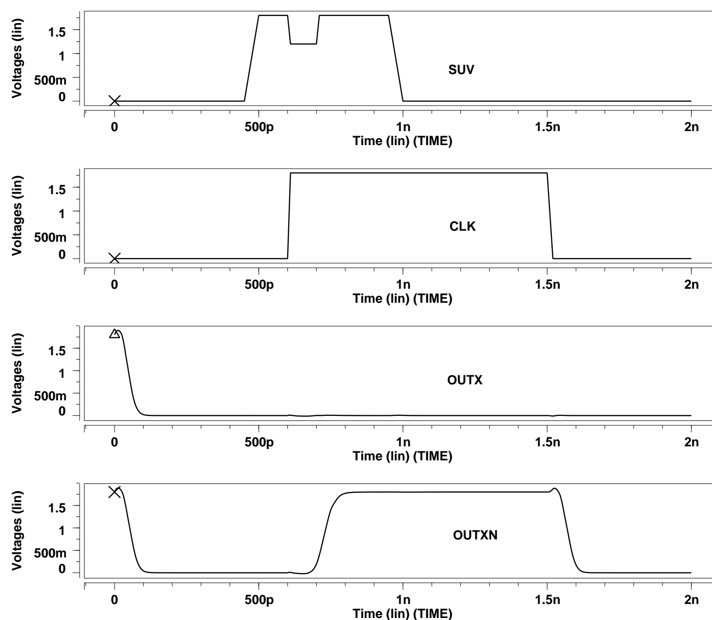


Figure 3.10: Output response of the high level SIV monitor when a SIV occurs.

For the high level monitor, those undershoots below V_{DD} with NW and NH values located above the curve are detected. Those located below the curve are not detected. Undershoots of small duration require a higher NH in order to be detectable. The detectable NH of the undershoot is lower as the NW increases. For a sufficiently large undershoot duration the required NH does not increase for larger NW. For the designed monitor the minimum detectable NW is 10ps.

The performance of the monitor can be further improved. The sizes of the

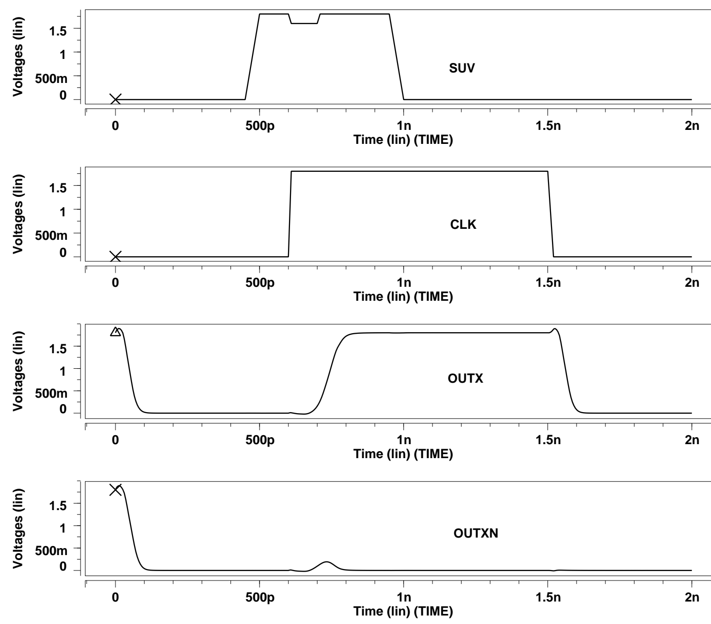


Figure 3.11: Output response of the high level SIV monitor when a SIV does not occur.

pre-charge transistors can be minimized for reducing the load at the nodes X and XN. Also the sizes of the latch transistors can be optimized for improving speed. Moreover minimizing the channel length of t_{l1} and t_{l2}, their channel width is optimized to assure the positive feedback for the monitor. The behavior of the low level monitor is similar to the previously described monitor. Its performance is shown in Fig. 3.13. Again two regions are well defined, the detectable region and the undetectable region.

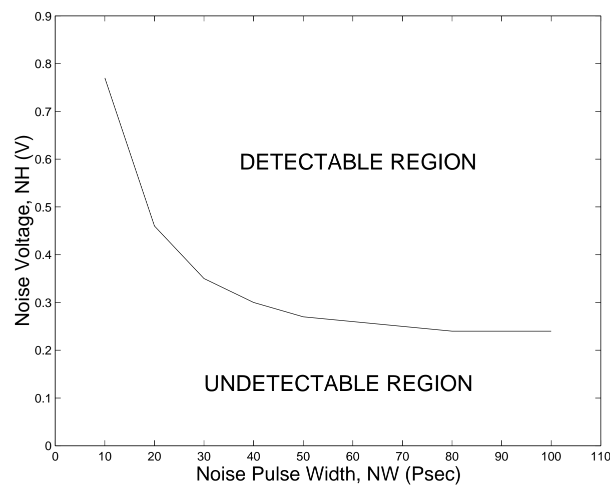


Figure 3.12: Pulse width duration of the noise versus voltage noise for the high level SIV monitor

The curves shown in Fig. 3.12 and Fig. 3.13 can be modified by design in order to satisfy the noise margin requirements for a specific gate. For example, if a gate has the noise margin characteristics shown in Fig. 3.14(b), all noise voltage into the undetectable region will cause false switching in that gate (inverter B in Fig. 3.14(a)). If the gate has the SUV as its input the unacceptable noise can be detected by the proposed monitors. In order to detect all these unacceptable noise, the performance curve of the monitor should be placed into the unacceptable noise region of the gate that is receiving the signal under test. The detectable and undetectable noise region can change due to process variation. Because of this, an uncertainty region is present in the noise margin regions, this region is analyzed later.

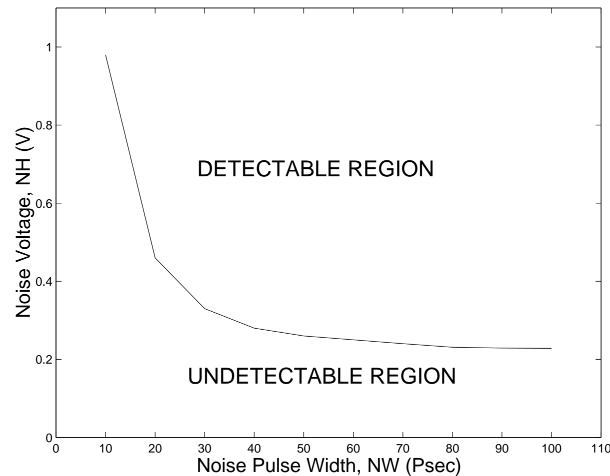


Figure 3.13: Pulse width of the noise versus voltage noise for the low level SIV monitor

Fig. 3.15 shows curves for high level monitor performance for different ratios of transistor *Tin1* and *Tin2*. Changing the ratios of the input transistors is possible to move the monitor performance curve in order to establish the adequate detectable region.

3.4 Coherent sampling

Today, products as high bandwidth on-chip systems, high speed transceivers, etc., that runs at rates of gigahertz are required. Testing internal signals of these products is a current challenge due to the high signal rate and low signal swings. Custom instruments are needed to achieve the verification of these signals but they are prohibitively expensive for high volume production [100] [98]. Sampling a higher frequency signal using conventional Nyquist sampling would require over twice the sampled signal frequency. This is inviable if the sampled signal frequency is in the limit of the frequency obtained by the current technology. The solution is to sampling the signal under verification (SUV) at rates that are less than the SUV frequency. The result is a downconversion of the sampled signal, it means that all signal information are retained but at a lower frequency.

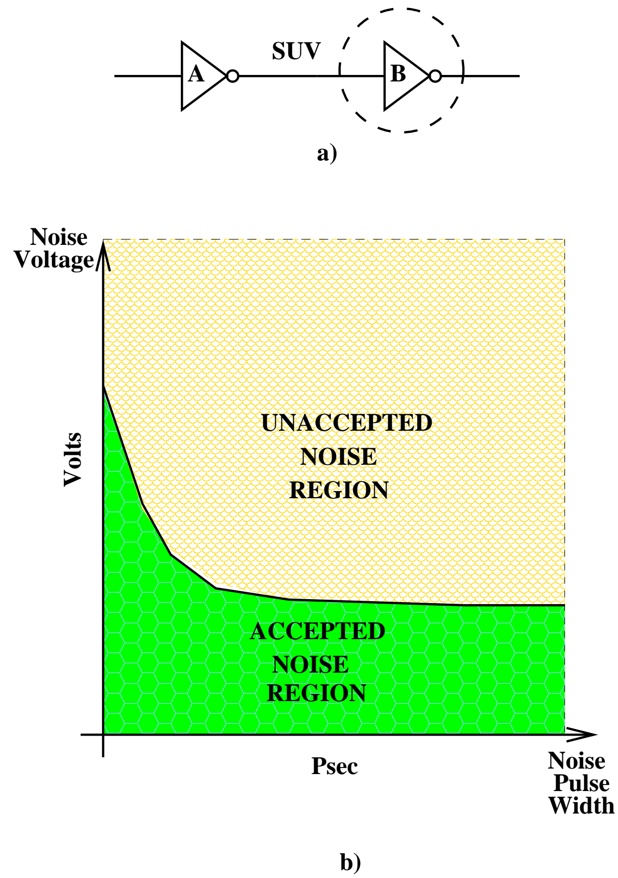


Figure 3.14: Example of an inverter noise margin curve showing the regions of acceptable and unacceptable noise voltage.

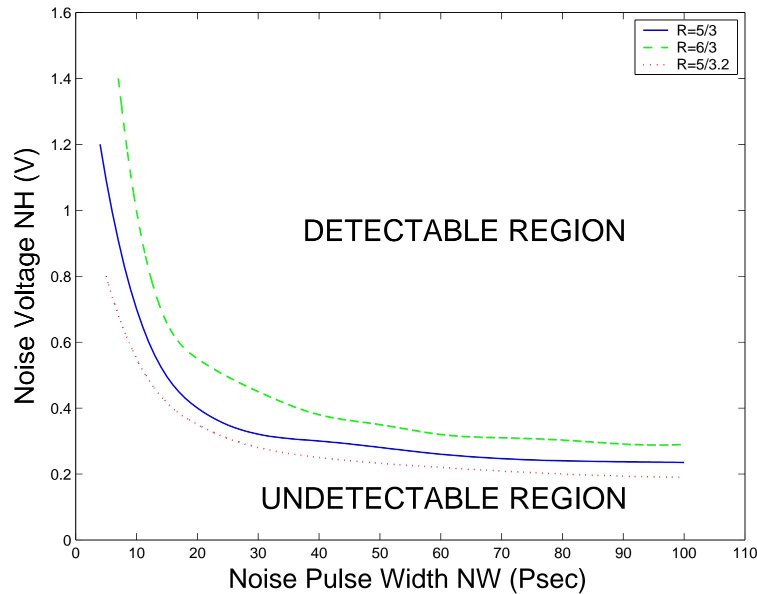


Figure 3.15: Pulse width of the noise versus voltage noise for different ratios of the inputs transistor widths for high level SIV monitor

A special relation between the sampling and sampled signal is needed in order to obtain the desired information without aliasing. This relation is obtained by choosing two relative integer prime number in order to get a "coherent" relation between sampling and sampled signals. If the coherent relation is achieved an effective frequency results that is greater than twice the sampled signal frequency is obtained. The required resolution of the sampling signal is set-up by the relation of these two relative integer prime numbers which for this analysis are called M and N. The sampling technique using this relation is called "coherent sampling".

In coherent sampling [97][100][98], the effective sampling rate is governed by Nyquist principle and not the actual sampling rate (See Fig. 3.16). The coherence relation is:

$$\frac{F_t}{F_s} = \frac{M}{N} \tag{3.1}$$

Where

- F_t is the frequency under test

- F_s is the sampling frequency
- M is the integer number of cycles of the signal under test that form a unit test period (UTP)
- N is the number of samples taken in 1 UTP

In one UTP all the information is obtained in one period of the sampled signal. In the proposed methodology the sampled signal will be the signal under verification. This signal repeats M times into the UTP and N samples are taken. Into this UTP the high and low logic level of the signal under verification will be verified.

The amount of information available from a sampled waveform is maximized when M and N are relative primes. With this characteristic the amount of information is proportional to N and is independent of M. Coherent sampling enables to get all information of the signal in 1 UTP, the number of samples N in a periodic waveform should be sufficient to capture the total signal information. The effective sampling rate F_s' is given by eq. 3.2 [97],

$$F_s' = F_t \cdot N \ \ or \ \ F_s' = F_s \cdot M \tag{3.2}$$

A prime M/N ratio ensures that each cycle contributes unique, independent information. In coherent sampling it is not the current sampling spacing ΔT ($1/F_s$) that is important, but the effective spacing ΔT_P ($1/F_s'$). ΔT_P can be expressed in degrees as eq. 3.3 shows,

$$\Delta T_P = 360/N \tag{3.3}$$

In units of time ΔT is equal to

$$\Delta T_P = \frac{1}{F_s \times M} \tag{3.4}$$

When the coherent relation is established, it is possible to obtain all the required signal information. The signal under sampling repeats M times (one UTP) and N samples will be taken in one UTP.

3.4.1 Scheme of coherent sampling

In order to clarify the above theory, a basic scheme of coherent sampling is presented. In coherent sampling, the sampled signal corresponds to the all

signal information to one period of the signal under sampling as depicted in Fig. 3.16. The coherent relationship will work for any arbitrary M and N, but practical values provide better results. A prudent choice for N is a power of 2. The fast Fourier transform (FFT) requires the number of samples to be a power of 2 because of its inherent periodicity. M should be odd or prime. By making M odd many common factors with N are eliminated. When N is a power of 2, any odd number for M is relatively prime with N. Common factors between M and N lead to different harmonics of SUV having the same frequency in the FFT after aliasing [101].

In a periodic waveform, coherent sampling is used to cover all signal in-

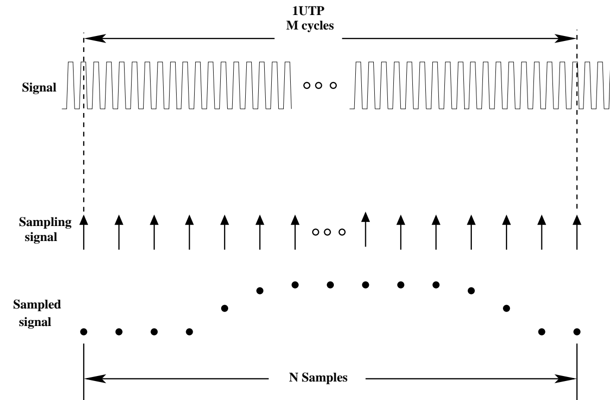


Figure 3.16: Basic scheme of coherent sampling where N samples are taken of a signal that repeats M times

formation [97]. For example, for a 1 GHz signal under verification (SUV) and a coherent ratio, $\frac{M}{N} = \frac{1023}{256}$ are necessary for a coherence sampling signal at $F_s = 250.244MHz$ where this F_s signal corresponds to an effective sampling $F_s' = 256GHz$. It means that in 1 UTP = 1023 cycles, of the signal under test, 256 samples will be taken. Each sample will have a different value of the signal under test with an effective spacing of 3.9062ps. In order to show coherent sampling signals, the circuitry shown in Fig. 3.17 is used as example. The circuitry has a type D flip-flop with CLK input as the sampling signal at coherent frequency F_s, the SUV is the D input of the flip-flop. The flip-flop output Q is the sampled signal that corresponds to one period of the SUV.

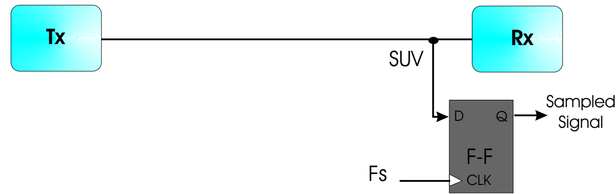


Figure 3.17: Circuitry for taken a coherent sampling

The signals representing this example are shown in Fig. 3.18. The upper panel displays a squared signal at frequency of 1 GHz (SUV). This signal must be taken at the input of receiver (Rx on Fig. 3.17). The middle panel exhibits the sampling signal at coherent frequency F_s, this signal is the CLK input of the flip-flop. Since the flip-flop stores the signal on its input at the moment when CLK is high, the output Q (lower panel) will be the sampled signal at frequency F_s.

The desired coherent frequency could be obtained from a master CLK.

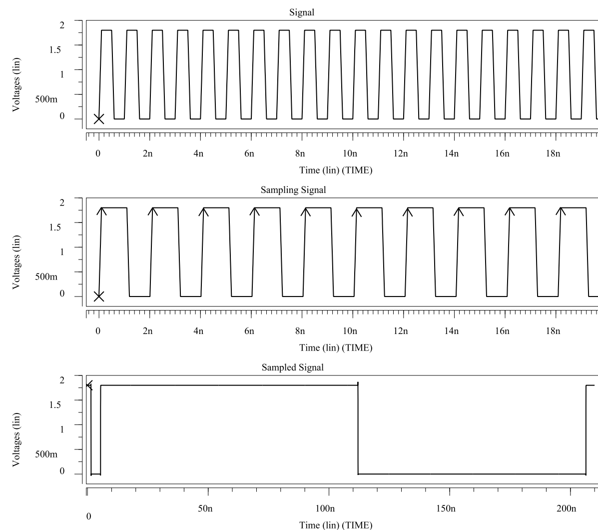


Figure 3.18: Example of coherent sampling

In practice the duration of the sampled signal is fixed, hence the coherent sampling signal can be generated by a PLL circuit as Fig. 3.19 shows. This

structure is usually included in modern processors. The desired coherent relation can be achieved by dividing by M and by N counters [100]. The CLK signal generated by coherent Sampling is used to obtain information of the SUV and to generate the enable signals for the monitors as is shown in the next section.

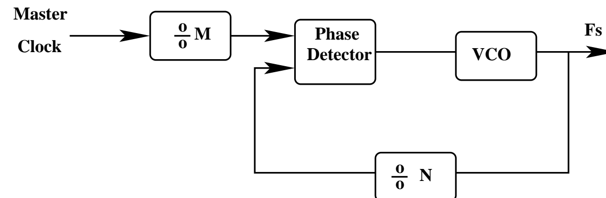


Figure 3.19: Coherent sampling generator

3.5 Monitoring system architecture

The monitoring system architecture using monitors (high and low) for verifying n-signals is presented. In addition, it should be assure that these is no loss of information of the sampled signal. Furthermore, our test strategy has flexibility for selecting the desired coherence relation. Two monitors, one for the high level and the other for the low level, are used. Signals need to be generated to enable proper selection of the monitors for each signal to verify. Fig. 3.20 shows the enable signal generator needed for sensing n signals (where n=1,2,3...etc.). The monitor selector generates the signal ER by sampling the SUV at the CLK frequency. The signal ER is used to determine which monitor output will be stored by the monitor output analyzer. If ER is low (high) the monitor output analyzer stores the low (high) level monitor output. The information stored by the monitor output analyzer is sent to an output pin. The signal ER is also used by the enable signal generator. The enable signal generator receives the ER and CLK signals and generates the enable signals for the high and low level monitors. The number of enable signals depends on the number of the signals to verify. For example, three enable signals are required to verify three signals per monitor.

During one UTP window, one SUV is verified for overshoots/undershoots in the low/high level of the signal. The enable signal generator is able to

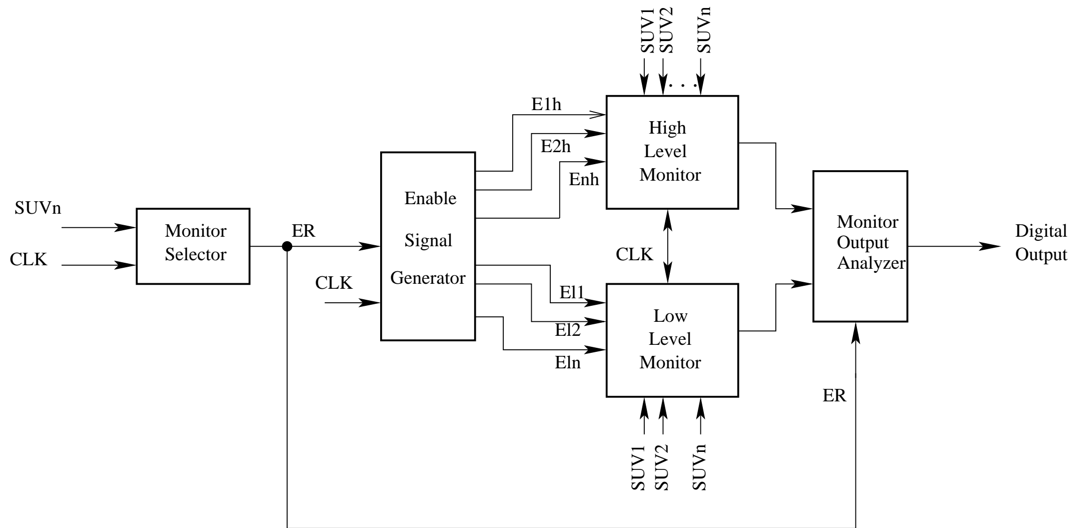
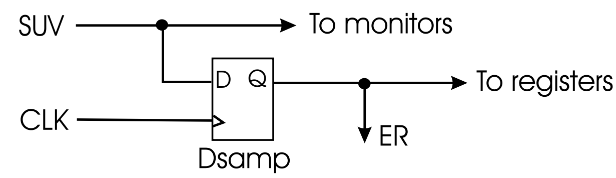


Figure 3.20: General scheme of the monitoring system architecture. Enable signals are generated for each monitor. Signal ER controls what monitor output will be analyzed.

identify when the high(low) logic level of the SUV has been verified in order to set the high (low) level monitor ready to verify the next SUV in the high(low) logic level in the next UTP window.

3.5.1 Monitor Selector

The high (low) level monitor output is stored by the monitor output analyzer when the logic value of ER corresponds to the high(low) logic state of the SUV. The proposed circuit for doing this task is shown in Fig. 3.21. The flip-flop ***Dsamp*** takes samples of the SUV at CLK rate. The signal CLK has the coherent sampling frequency that also feeds the monitors. The signal ER allows to know which logic level of the SUV is being evaluated by the monitors in each CLK period. The output of ***Dsamp*** (ER) has the logic values of the SUV at the moment of sampling. For example, if the logic value of ER is 0 (1) means that the SUV is being evaluated at its low (high) logic level (See Fig. 3.21). Hence, the low level monitor output must be stored in the monitor output analyzer. When ER is low (high), the stored element of the low (high) monitor output is activated. The information in ER is also useful for the enable signal generator as is explained in the next



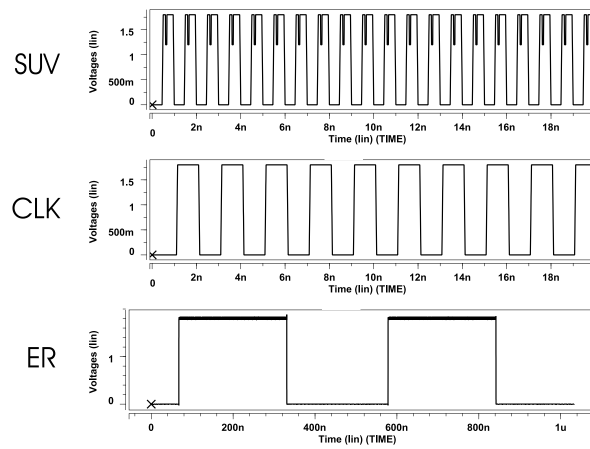


Figure 3.21: Behavior of the monitor selector

subsection. Fig. 3.22 shows two possible cases of ER. These cases depend on the first sample taken on SUV. Case I (Fig. 3.22(a)) occurs when the first sample is taken in the low level of SUV. Hence, the first value of ER is low. The first logic change of ER will be from low to high. The second logic change of ER indicates the end of the ER high level, which means that the SUV has been verified in its high logic level. The third logic change of ER will be from low to high and indicates the end of the low level of ER. In this point the low logic level of the SUV has been verified. In the case II (Fig. 3.22(b)), the first sample is taken in the high logic level of the SUV, the ER logic values will be complementary for the Case I. Note that three ER transition changes are required to verify the high and low logic level of one SUV. Hence, to pass to another SUV is needed to know when ER has had three transition changes. The enable signal generator achieves that function.

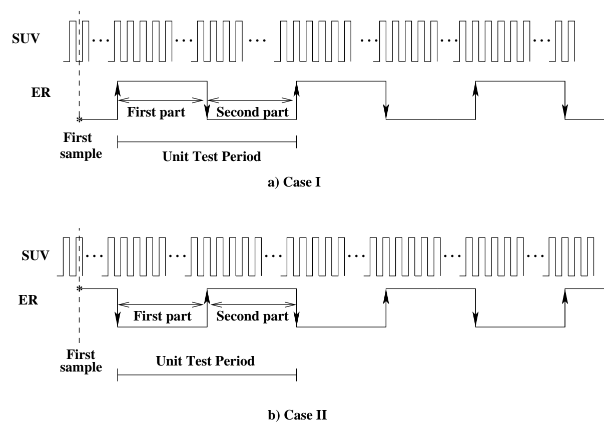


Figure 3.22: Sampling Flip-Flop and timing curves for the cases when the first sample has logic value of 0 or 1. Because the unknown logic value of the first sample of SUV, two cases arises.

3.5.2 Enable signal generator

The main function of the enable signal generator is to produce the enable signals for the high and low level monitors in order to verify the SUV in one UTP window without loss information. Because the monitors are capable to verify several signals, the enable signal generator must be able to identify

the end of one UTP, and generate the corresponding enable signals to verify the next signal in the following UTP. Fig. 3.23 shows the block diagram of the enable signal generator. The enable signal generator uses the signal ER

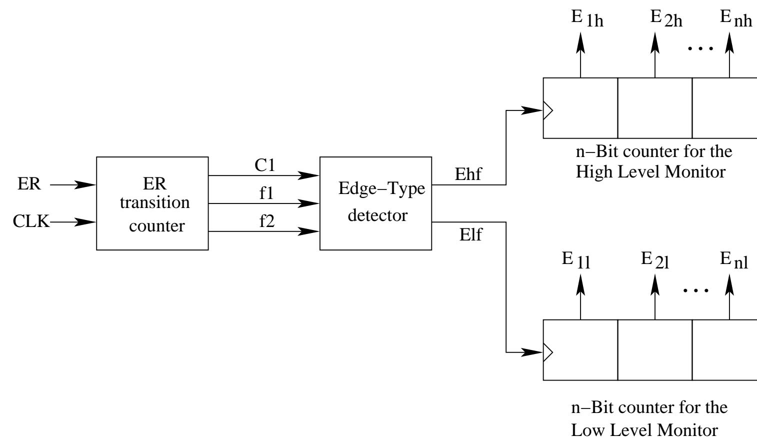


Figure 3.23: Block diagram of the enable signal generator.

and CLK to generate the enable signals. The ER transition counter counts the logic transitions of the signal ER in one UTP. This count allows to know when the high/low logic part of the SUV has been verified and also when one UTP has finished. For example, if the first logic value of ER is a logic 0 (See Fig. 3.22(a), the first transition of ER is from low to high and the second one from high to low. Hence, when two ER transitions have been counted, this means that the high logic level of the SUV has been verified. The third transition of ER indicates that the low logic level of SUV has been verified by the low level monitor and also that the UTP window for that SUV has finished. The Edge-type detector identify if the ER transition has occurred from high to low or low to high. This helps to determine what logic part of the SUV has been verified. The n-bit counters for the high and low level monitors produce the signals that enables the high and low level monitors to verify the corresponding SUV. E_{hf} and E_{lf} signals indicate which n-bit counter must change its state.

Strategy to generate the enable signals

In the first UTP is verified SUV1, in the second UTP is verified SUV2 and in the nth UTP is verified SUVn. The enable signal generator (Fig. 3.23) indicates to the monitors which SUV must be verified in the corresponding UTP. In the first part of a UTP is verified the high or low logic level of the SUV, and in the second part of the same UTP is verified the other logic level of the SUV. Because the signals to enable the monitors are generated using SUV and CLK (sampling signal), the first sample of the second signal under verification is lost (See Fig.3.24). This figure shows that the end of UTP1 is the beginning of the UTP2 and this condition is detected at time $tx1$. At this time the low level monitor should be verifying SUV2 but it does not happen because the enable signals corresponding to SUV2 are still changing to its final logic value. Hence, the first sample evaluation of SUV2 is lost. The same situation occurs for SUV3 at time $tx2$ and so on.

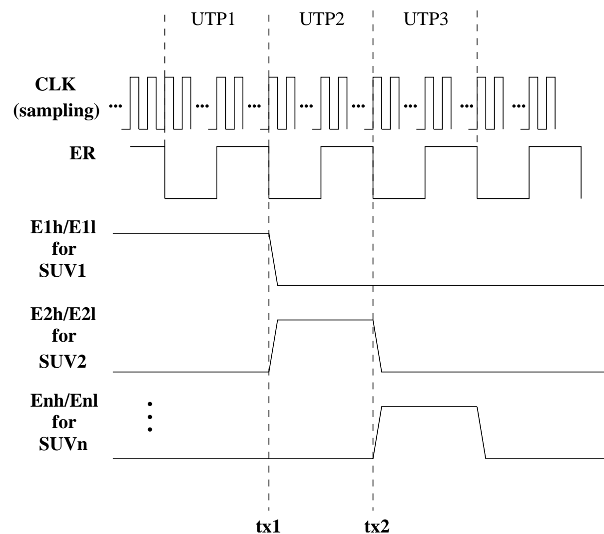


Figure 3.24: Enable signal set to verify three different signals. The step to change from SUV1 to SUV2 and then SUV3 occurs with loss information in $tx1$ and $tx2$, because just at these time the enable signals E_{2h} and E_{2l} are activated

Without loss of generality, let's consider three signals to verify for explaining how this issue is solved. In this case the enable signal generator

produces three enable signals for the low and high level monitors. The values of these signals are controlled by the flag signals E_{hf} and E_{lf} as shown in Fig. 3.25(a). Each time that there is a 0 to 1 transition at E_{hf} (E_{lf}) the shift register is moved one position to the right. The different values of the enable signals and the corresponding states of the shift registers are shown in Tables 3.2 and 3.3. The corresponding signal under verification (SUV) is also shown in the third column.

$E_{1H}E_{2H}E_{3H}$	STATE	SUV
1 0 0	S_1^H	SUV1
0 1 0	S_2^H	SUV2
0 0 1	S_3^H	SUV3

Table 3.2: Shift register state for the high level monitor. For each state corresponds one SUV.

E_{1L} E_{2L} E_{3L}	STATE	SUV
0 1 1	S_1^L	SUV1
1 0 1	S_2^L	SUV2
1 1 0	S_3^L	SUV3

Table 3.3: Shift register state for the low level monitor. Each state enables to low level monitor to verify one SUV.

Let's consider a high to low transition of ER (See Fig. 3.25(b)). The state of the shift register for the low (high) level monitor is S_1^L (S_1^H). As a consequence the low level part of SUV1 is verified, and it is enabled (but not verified) also the high level monitor for SUV1. The second transition of ER (0 to 1 transition) indicates that the verification of the low level of SUV1 has finished. The state of the shift register for the low (high) level monitor are S_2^L (S_1^H). As a consequence the high level part of SUV1 is verified, and it is enabled (but not verified) also the low level monitor for SUV2. The third transition of ER (1 to 0 transition) indicates that the verification of the high level of SUV1 has finished. The state of the shift register for the low (high) level monitor are S_3^L (S_2^H). As a consequence the low level part of SUV2 is verified, and it is enabled (but not verified) also the high level monitor for SUV2. This process continues until to verify the high and low logic levels of all the signals.

Next, the circuit implementation of this strategy is presented.

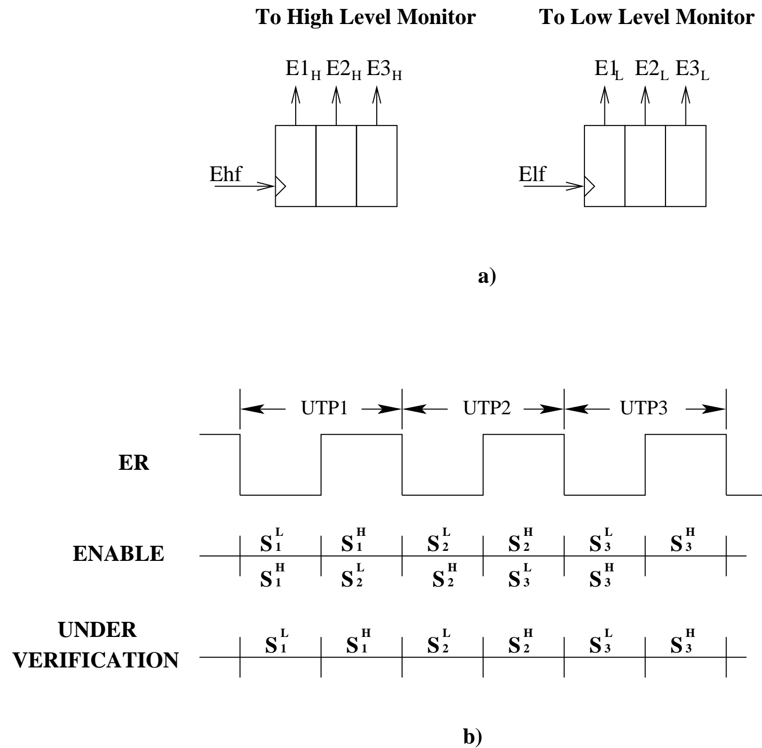


Figure 3.25: Shift register used as enable signal generator to the high and low level sensing monitors.

Implementation of the enable signal generator

Fig. 3.26 shows the circuit implementation of the enable signal generator. Timing curves depicted in 3.27 allows to understand the performance of the overall enable signal generator.

First the ER transition counter module is described. Let's assume the case of the ER signal shown in Figure 3.27. The output of the X-OR gate produces a pulse at each ER transition. The 2-bit counter makes a count at each pulse. HSB and LSB take the values shown in Figure 3.27. The initial values of HSB and LSB are 01. Then, they change to 10, and 11. In this way a UTP period is recognized. The HSB and LSB values are reseted each time

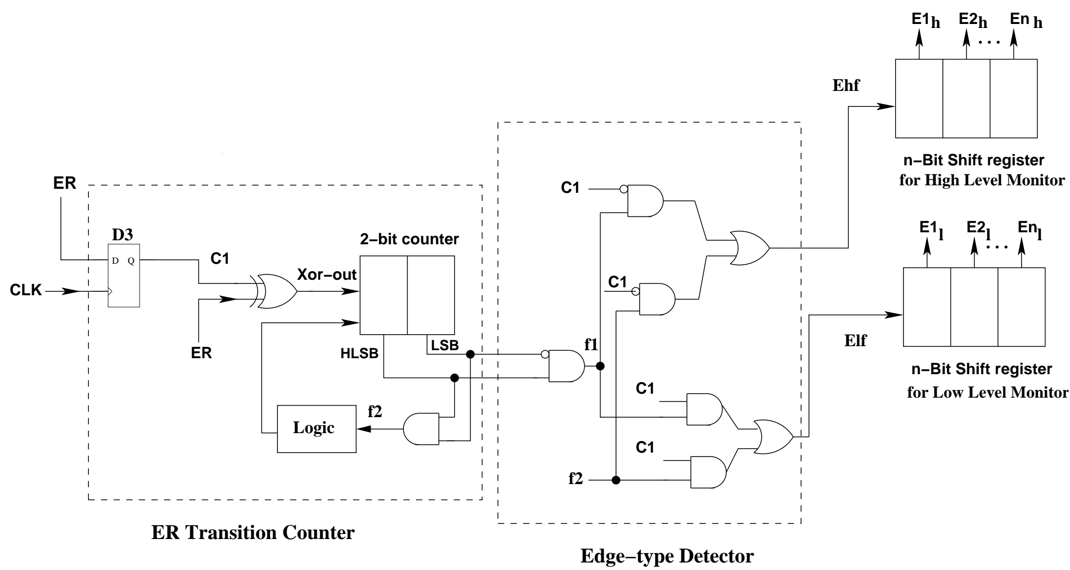


Figure 3.26: Schematic circuit of the enable signal generator.

that a UTP period ends. When the 2-bit counter has the count 11, other logic change of ER indicates that a complete UTP has finished and the next signal will be verified. At this moment the respective enable signals for the next UTP must be generated. When the 2-bit counter computes the binary number 11, the signal f_2 (See Fig. 3.26 becomes high by the action of the AND gate connected to the two-bit counter outputs. The signal f_2 produces a high logic level at the output of the AND gates (E_{lf} or E_{hf}) only if C_1 or $\overline{C_1}$ is high. The 2-bit counter must be reset to the count of 01 just in the CLK period after the count of 11.

The edge-type detector (See Fig. 3.26) identify if the transition of ER was from 1 to 0 or from 0 to 1. In the case of the count of 10, the detection is achieved by an AND gate which has the inputs connected at the 2-bit counter outputs (Fig. 3.26). When the 2-bit counter computes the binary number 10 (2 decimal), the AND output f_1 becomes a logic one. This output feeds one input of other two 2-input AND gate which outputs will activate the clock input of the n-bit shift register. Hence, it generates the enable signals for the high or low level monitors depending on the direction of the transition of ER. The second input of this two 2-input AND gate is the signal $\overline{C_1}$ and for the other AND is C_1, the outputs of these AND gates (E_{hf} and E_{lf}) will be high only if the signal f_1 and C_1 or $\overline{C_1}$ are high. The signal

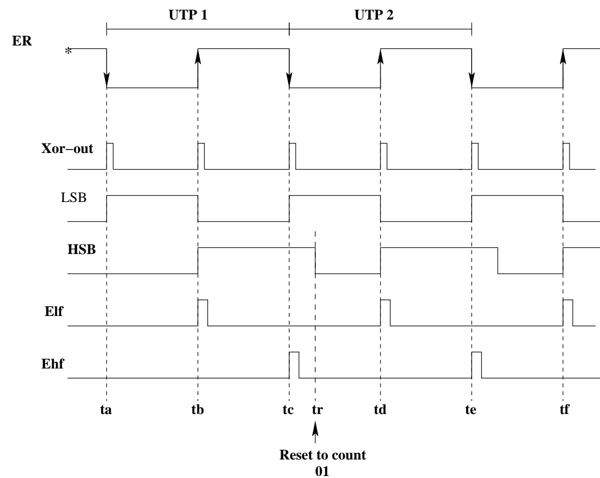


Figure 3.27: Timing curves showing the performance of enable generator.

E_{hf} (E_{lf}) activates the n-bit shift register for the high (low) monitor (See Fig. 3.26) which activates the enable signal to verify the corresponding SUV.

Fig. 3.28 shows the electrical simulation of the enable signal generator. The signal E_{hf} is set to a high logic level when the two-bit counter counts the binary number **10** and the change of the signal ER is from high to low. The signal E_{lf} is set to a high logic level when the two-bit counter counts **11** and the signal ER changes from low to high. The circuit implementation of the two-bit counter is shown in appendix A.

3.5.3 Monitor output analyzer

When the monitors receive the CLK signal, they evaluate the integrity of the SUV, their outputs are digital signals that need to be processed. Because the signal integrity verification (SIV) need two monitors, one for undershoots and another for overshoots, it is necessary to identify when the signal under verification (SUV) is in the high or low logic level in order to store the monitor output in a register (see Fig. 3.29). The latch D_{samp} are used as a sampler at rate of CLK (the sampling frequency), this latch captures the SUV at the moment when CLK is high, its output (ER) is used to enable the register that stores the monitor output. For example, if the signal Er is low (high) the flip-flop assigned for storing the output of the low (high) level monitor is

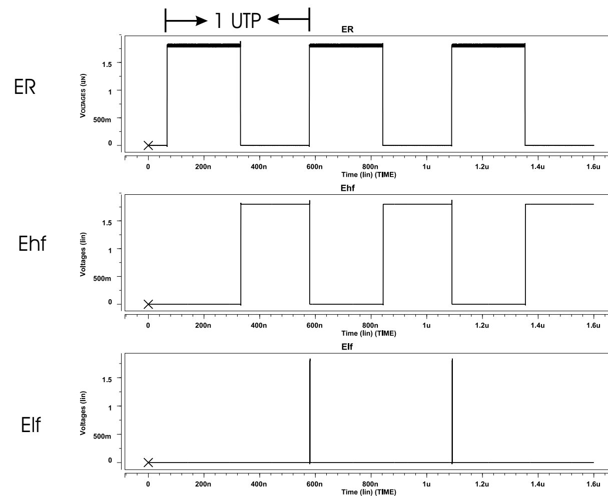


Figure 3.28: Simulation of the enable signal generator. The signal E_{hf} goes to high when the the signal ER changes from high to low and the signal E_{lf} goes to high when ER changes from low to high.

enabled. The latches *Dh* and *Dl* assure to store the data each CLK cycle.

3.6 Methodology accuracy

In this section, those condition affecting the accuracy of the proposed methodology are analyzed. In other words, when the SIV could not be detected. One cause for do not detecting a SIV is the proper monitor performance. As shown shown in Figs. 3.12 and 3.13, the monitor response depends on the voltage level and duration of the noise pulse. For example, if the noise pulse duration is smaller than 5ps the monitor designed in a 0.18μm technology fails to detect the noise pulse, because the monitor only detects noise pulse durations above 10ps (see Figs 3.12 and 3.13).

Several samples of the signal under verification (SUV) are taken by a sampling signal at coherent frequency. As it was explained before, the effective sampling gives the resolution of the sampled signal. Fig. 3.30 depicts some samples taken to the SUV in the part where the undershoots take place. The shadow area of the undershoot is the noise voltage level that the high level monitor could detect. Three samples fall in this area (t_3, t_4 and t_5) and in

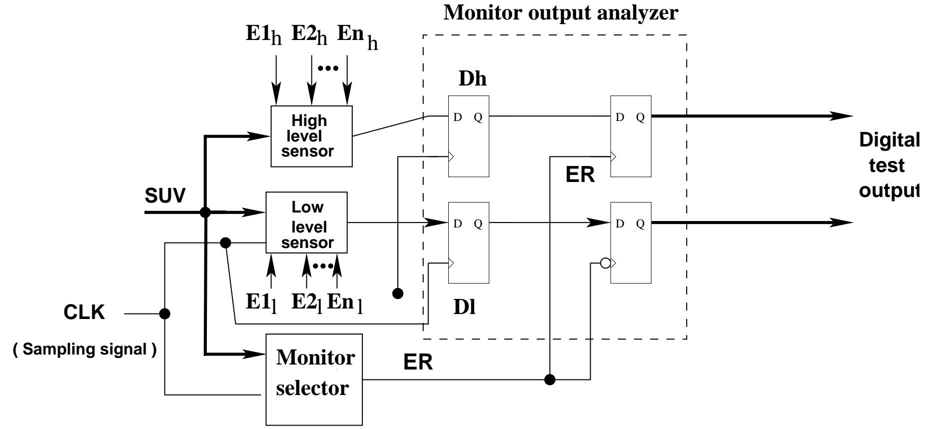


Figure 3.29: Methodology for monitor output analysis

these samples the monitor will detect the SIV. Also, due to the monitor response time t_{mr}, it is possible that the last sample into the detectable region could not be seen by the monitor. t_{mr} is the time required for the monitor to evaluate a signal sample value. This t_{mr} is $3ps$ for a monitor designed by using a $0.18\mu m$ technology. The resolution established by the coherent sampling allows to obtain more than three samples into the detectable region.

Hence the detectable region (DR) can be defined by

$$DR = NW \tag{3.5}$$

Where NW is the noise width duration into the detectable region. According with the effective sampling the detectable region can have K samples, for this example $K = 4$ because the sample in t_2 is included by the action of the t_{mr} and the last sample in t_5 into the DR is still detected. Also it is possible to say that the resolution in time of the sampling is

$$r = \frac{DR}{K} \tag{3.6}$$

Resolution value will be equal to $t_2 - t_1$ or $t_3 - t_2$ for this example, and also in the general case. Clock jitter is a source of possible errors in this methodology, therefore it is important to estimate the total amount of the jitter allowed in order to assure the detection of a SIV. The jitter of the signal under verification also affects the detection of the signal noise. Both jitters

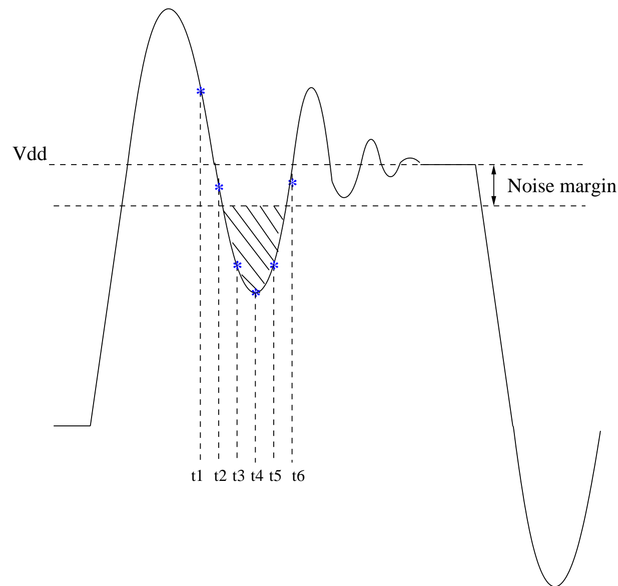


Figure 3.30: Samples taken in the undershoot area are shown the resolution of the effective sampling frequency.

are depicted in Fig. 3.31. In this figure the CLK and SUV jitter are shown.

Let's consider that the last sample taken was in t_1, the signal jitter can cause the sample taken in t_2 does not fall into the detectable region. Also the clock jitter can affect the sample taken in t_2, where due to jitter, the sample taken is out of the detectable region. Both jitters must be considered in order to assure the detection of a signal integrity violation.

Total jitter accumulated must be smaller than the detectable region as indicated by (3.7):

$$\Delta T_{jitter} < NW \tag{3.7}$$

Equation (3.7) is a general condition and it is necessary to establish the total amount of jitter allowed in order to assure the detection of the noise pulse. The condition given by equation (3.8) assures that almost one sample will be taken into the detectable region despite the total accumulated jitter, and therefore the SIV will be detected by the monitor. Aperture jitter in the 0.5-2ps range is typical for high performance electronics (A/D converters for example) [102], this means that signal with relatively low jitter can be

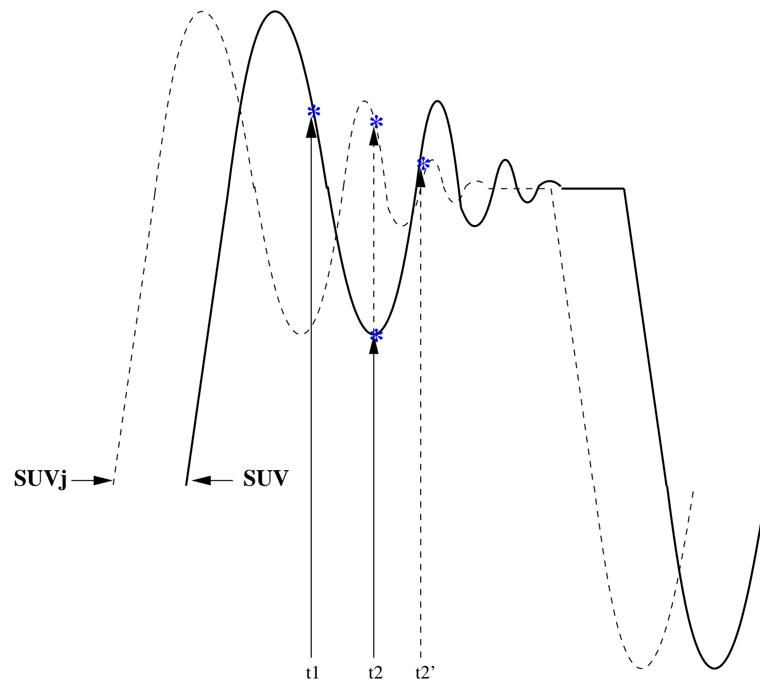


Figure 3.31: Jitter issue affecting the signal integrity verification methodology.

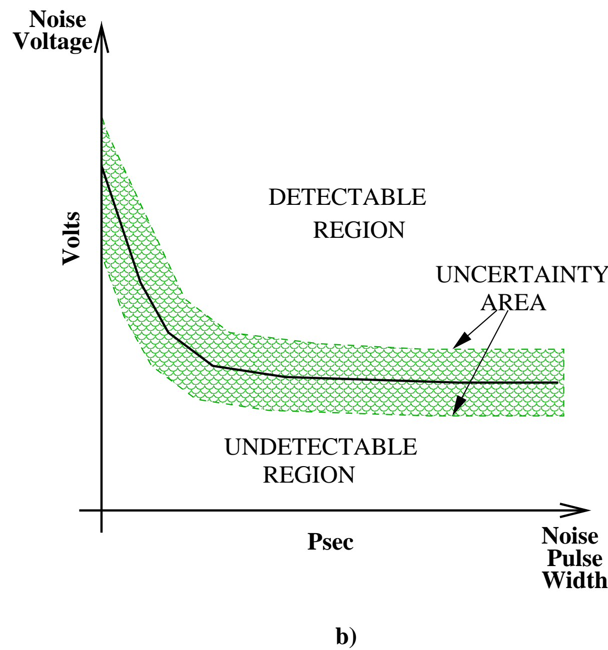


Figure 3.32: Process variation impact over the performance curve of the monitor

obtained in current technologies, however limits of jitter values should be established to assure a good performance of the methodology.

$$\Delta T_{jitter} = (K - 1)r \tag{3.8}$$

The signal under verification (SUV) can suffer of jitter but, in combination with the clock jitter, the total amount of jitter accumulated should be equal or smaller that the amount established by equation (3.8).

Process variations can also affect the methodology accuracy; the performance curve of the monitor could be affected by modifications caused by the fabrication process as Fig. 3.32 shows. The shadow area in Fig. 3.32 shows the possible variations of the performance monitor curve due to process variation. These variations can affect the accuracy because the detectable region for which the monitor was designed can change drastically. It is important to take into account the possible deviations of the performance curve in the design stage. As a example, the data depicted in the monitor performance curve in Fig. 3.12 may present, due to process variations, data dispersion.

It is possible to estimate standard deviation of the total points obtained by Montecarlo analysis. The standard deviation is given by

$$\sigma = \sqrt{\frac{n\sum x^2 - (\sum x)^2}{n^2}} \tag{3.9}$$

Where σ is the standard deviation, n is the number of data, and x is the data value average. σ represents the dispersion of the values with respect to the average. For the data of the Fig. 3.23 the standard deviation is $\sigma = 0.52$.In order to assure detectability according with the specifications it is important to take into account this value at time of design.

3.6.1 Cost of the proposed verification methodology

The cost of the proposed verification strategy has been estimated in terms of area, extra pins and delay penalization. Two monitors are required. Considering three signals to be verified, the estimated area for these monitors is $274\mu m^2$ by using a 0.18 μm technology. The estimated area for the monitoring system architecture is $2032\mu m^2$. If the sampling signal is generated internally, the required area for the dividers must be included. These dividers are required to obtain the coherent relation $\frac{M}{N}$.

An extra output pin is required. It is required to send out the stored information given by the monitors. Because the monitor output is stored in a flip-flop, the flip-flop information could be sent out serially by that pin. For each sensing line the added capacitance due to the input gate capacitance of the sensing transistor of the monitor is about 4.4 fF. Assuming a transmission line of length of 1 mm which is handled by a driver and with a similar load at its end, the added delay due to monitor connection is 4ps. The Fig. 3.33 shows the delay impact for adding the monitor. Table 3.4 indicates the delay impact for adding the proposed methodology. The delay contribution of the verification circuitry has been examined for different interconnect lengths. The required time to verify one signal depends on the duration of the unit test period (UTP). The coherent sampling frequency determines the UTP duration. For example, the duration of the UTP to verify a signal (SUV) with frequency of 1GHz is 507 nsec. This time is obtained if 128 samples are taken to the SUV in 507 periods of the SUV. The required time to achieve the verification is increased when the number of the signals

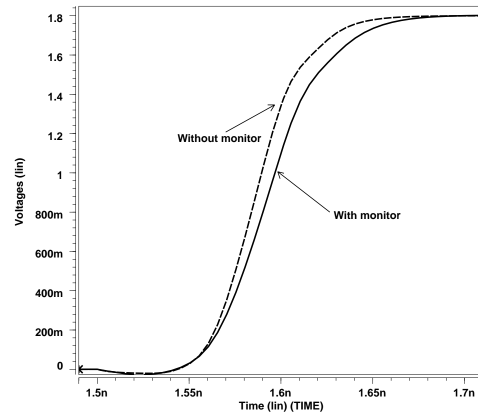


Figure 3.33: Delay added by monitor connection. l=1mm.

l(mm)	Added delay
0.5	2%
1	7.1%
2	13.6%
3	13.5%
4	11.5%
5	8.8%
10	3.4%

Table 3.4: Delay impact of the proposed methodology. The percentage values are the delay contribution by adding the verification methodology.

to verify is increased. Verifying three signals at the same frequency, 1 GHZ for example, three UTP are required. Hence, the required time is 1.521 μsec. Note that the methodology test time have a direct relationship between the required M periods to take the N samples of the SUV and the number of the SUV to verify. The required verification time (T_{ver}) can be calculated by the following expression:

$$T_{ver} = M * T_{SUV} * n \tag{3.10}$$

Where M is the required number of SUV periods to take N samples, T_{SUV} is the SUV period and n is the number of signals to be verified.

3.7 Conclusions

The impact of interconnect effects on signal quality is relevant in high performance systems where high speed signals with good levels of integrity are required. Because of this, verification methodologies are required to assure proper digital signals. A new methodology for verification of the signal integrity violations has been presented.

Two monitors are proposed in order to sense signal undershoots and overshoots. The undershoots in the high logic level of the SUV are detected with the proposed high level SIV monitor. These undershoots could be seen as low logic levels for next stages that receive this signal as an input. Also, the overshoots in the low logic level of the SUV are detected by using the low level monitor. In both monitors, the threshold voltage detection is setup by the aspect ratios of T_{in1} and T_{in2}. The signals are verified under coherent sampling. The monitor response depends on the pulse width and height of the undershoots and overshoots. Two regions are well defined for both monitors, the detectable and undetectable region. When the NH decreases, the required NW increases allowing to detect a possible signal integrity violation. For a monitor with three input signals, the minimum detectable NW is 10ps by using 0.18 μm technology. The monitor performance can be further improved by reducing the loads at the nodes X and XN. Also, reducing the number of the signals, to be verified for the monitor, can reduce the loads in the nodes X and XN.

Each monitor can be used to verify more than one signal. The proposed

monitors allow the verification of critical signals where their quality is crucial to the performance of the system. The proposed test strategy allows to verify n-signals. Each signal is verified in one UTP. This is achieved by using an enable signal generator for each monitor. These enable signal generator allows to verify a signal in the high and low logic level in one UTP without losing information. These circuits also allow to pass from one SUV to another SUV without losing information. A two-bit counter and additional circuits are required to accomplish the enable signal generator.

The methodology accuracy is affected by the CLK and SUV jitter. Limits of jitter values are established to assure a good performance of the methodology. The signal under verification (SUV) can suffer of jitter but, in combination with the clock jitter, the total amount of jitter accumulated must be equal or smaller than the amount established by equation (3.8).

The cost of the proposed verification strategy has been estimated in terms of area, extra pins and delay penalization. The area required for the proposed methodology is $2300\mu m^2$. This area includes two monitors verifying three signals and the monitoring system architecture. An extra output pin is required. It is required to send out the stored information given by the monitors. For each sensing line the added capacitance due to the input gate capacitance of the sensing transistor of the monitor is about 4.4 fF. Assuming a transmission line of length of 1 mm which is handled by a driver and with a similar load at its end, the added delay due to monitor connection is 4ps, which corresponds to 7% of the total signal delay.

Chapter 4

Silicon Validation

In this chapter, silicon performance validation of the proposed verification methodology is described. Design and layout issues of the designed and fabricated circuits are given. Several blocks have been implemented to carry out the signal integrity verification inside the chip. The signal under verification (SUV) has been generated at different frequencies to have a spread of possibilities to show the feasibility of the proposed signal integrity verification methodology at different rates. AMI 0.35 μm CMOS technology has been used. This technology is used because has a reasonable cost. However, it allows to show clearly the feasibility of the proposed approach.

This chapter is organized as follows: section 4.1 describes the implemented circuits into the chip to accomplish the detection of signal integrity violations. The measurement results of the high level monitor are presented in section 4.2. In this section, the monitor results for evaluating the signal under verification (SUV), at different rates, and different coherent sampling rates are also shown. The section 4.3 presents the measurements results of the low level monitor. Here several results are exhibited at different rates of the SUV. An estimation of the duration of the noise pulse width injected to the SUV is described in section 4.4. Finally, in section 4.5, the conclusions of this chapter are given.

4.1 Circuits designed

All circuits have been designed by using AMI 0.35 μm CMOS technology under *CADENCE* environment and fabricated under the agreement with EUROPRACTICE. A photograph of the entire integrated circuit has been taken with an optical microscope (See Fig. 4.1). The modules used in the present work are marked.

The high and low level monitors have been designed individually in order

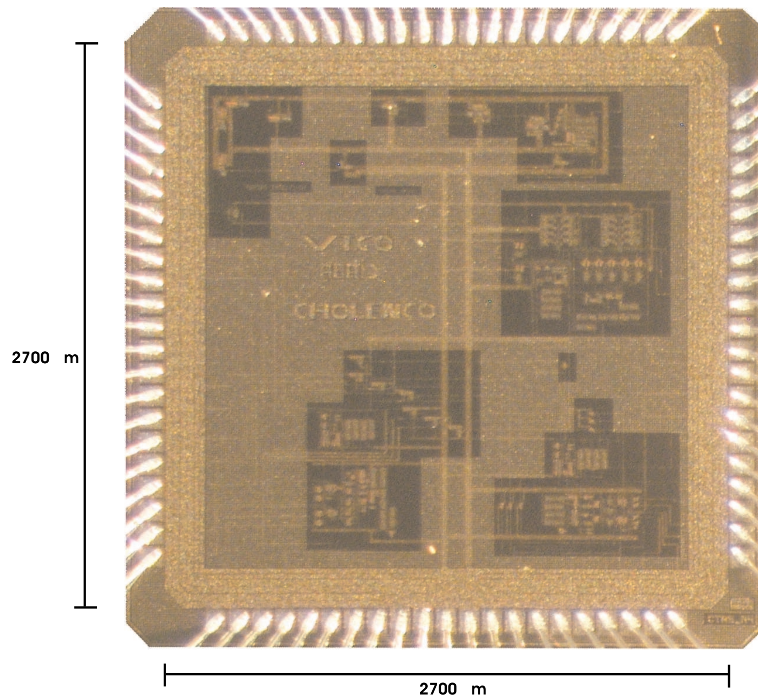


Figure 4.1: Photograph of the entire designed IC. The design area of the chip including the I/O pads are $8mm^2$.

to test their DC performance, all their inputs are connected to individual pads. Other block of the implemented circuits is the module with controlled frequency of the SUV. The module contains a VCO, frequency divider, noise injection circuit, selection circuitry to chose either the noise injected to the high or to the low logic levels of the SUV, and the high and low level monitors. Other implemented block is the module with a fixed high frequency of the SUV. The schematic circuits in this module are the same than for the module

of controlled frequency but each circuit has been redesigned in order to obtain the correct performance at this higher frequency (917MHz). Each circuit implemented in the chip will be described in the next subsections.

4.1.1 Monitors implemented for DC measurements

The high and low level monitors have been implemented individually to obtain their DC performance. The outputs (OUTX and OUTXN) shown in Fig. 4.2 goes directly to a PAD without buffer circuitry. The simulated (Hspice) DC performance of the monitors is obtained applying different DC voltages at their input (node **SH1** (**SL1**) in Fig. 4.2(4.4)) until finding the input voltage level for which the monitor is able to detect the minimum noise voltage. In this case the input DC voltage is the SUV. For completeness of the performance of the monitor, its dynamic behavior is required to be known. Because of this, let's describe next the dynamic performance of the high level monitor.

Fig. 4.3 shows the dynamic behavior of the high level monitor for dif-

Figure 4.2: Schematic of the high level monitor implemented to test the DC performance.

ferent noise pulse widths in the SUV. NH is the minimum noise voltage level which is detected by the high level monitor for a given noise pulse width (NW). The detectable and undetectable regions in Fig. 4.3 are obtained from the high level monitor which transistor dimension are shown in table 4.1. If those regions need to be different, T_{in1} and T_{in2} sizes must be changed.

Transistor	High monitor (W/L)
T_{p1}, T_{p2}	10/0.35
T_{l1}, T_{l2}	15/0.35
T_{eq}	10/0.35
T_{in1}	10/1
T_{in2}	5/1
T_b	20/0.35

Table 4.1: Channel width and length of the transistors of the high level monitor

A Monte Carlo analysis has been carried out for the monitor. The following tolerance parameters have been considered: 21% for the threshold voltage, 8% for the gate oxide thickness and 5% for the mobility. A parameter tolerance of 5% has been considered for the channel widths and lengths. The simulation results shown in Fig. 4.3 are obtained with 35 Monte Carlo runs. These Monte Carlo runs were applied in each NW point in order to find the lower and upper curves. For the lower curve, it was taken the NH values that generated at least one detection in a given value of NW in one iteration while in the other iterations the noise pulse was not detected. This operation has been made for each NW point of the lower curve. For the upper curve, it was taken the NH values that generate the monitor detection in all iterations in a given value of NW. This process was repeated for each value of NW of the upper curve.

Because variations of the process parameter occur, the upper (lower) limit of the detectable (undetectable) region goes upward (downward). As a consequence, only those points located above (below) the upper (lower) curve can be assured as detectable (undetectable). The noise height (NH) is almost constant for long noise widths. The DC performance of the high level monitor could be considered as a case of the longest noise pulse width of the SUV.

The minimum NH detected by the monitor in this case could be considered as the indicated by the typical curve on Fig. 4.3. The minimum NH detected by the high level monitor for the longest noise pulse width (700psec) in the typical case was 0.77V. This value could change by the action of process variations as it is shown in the upper and lower curves in Fig. 4.3. The regions can be modified by proper design of the channel transistor geometries of the monitor.

The individual low level monitor have been implemented to obtain simi-

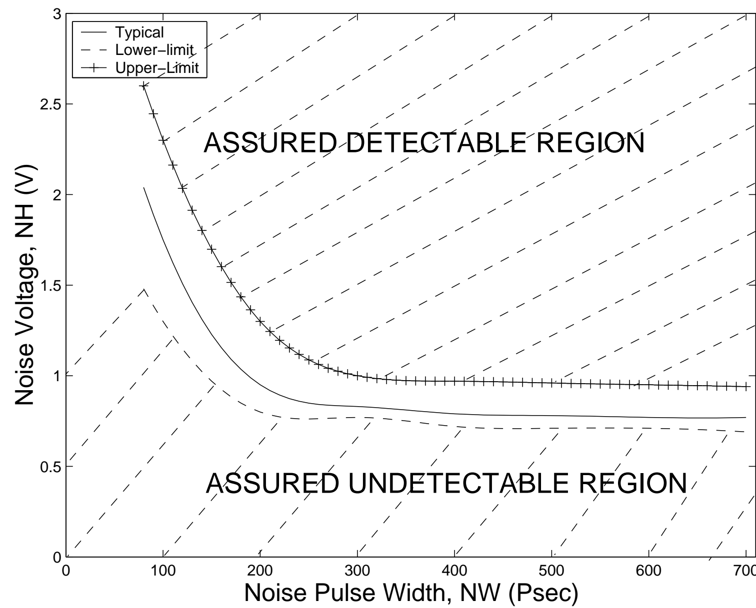


Figure 4.3: Pulse width duration of the noise (NW) versus voltage noise (NH) for the high level SIV monitor with transistor dimension shown in table 4.1. The assured detectable and undetectable region are shown. These regions were obtained by considering process variations.

lar results than those obtained with the individual high level monitor. The schematic of the implemented low level monitor is shown in Fig. 4.4.

The dynamic behavior of the low level monitor for different noise pulse widths in the SUV and for the transistor sizes shown in table 4.2 is shown in Fig. 4.5. NH is the minimum noise voltage level which is detected by the low level monitor for a given noise pulse width (NW). The transistor channel

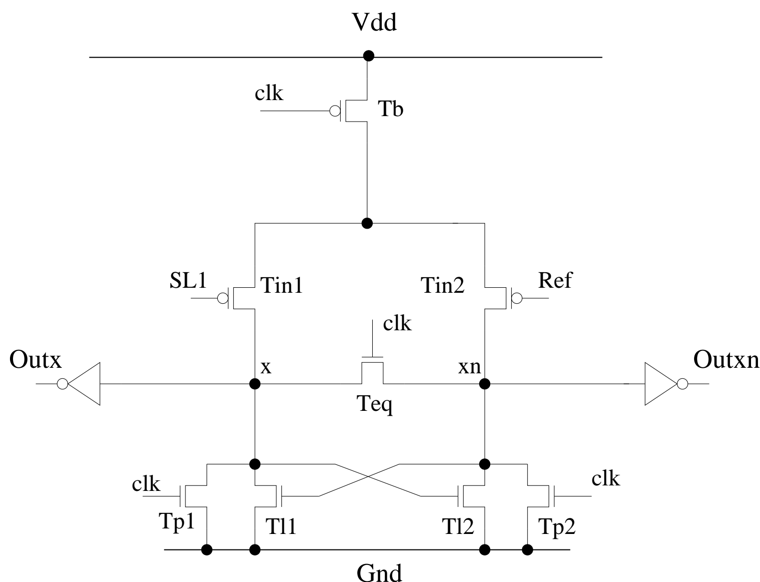


Figure 4.4: Schematic of the low level monitor implemented to test the DC performance.

widths of the designed monitor are given in table 4.2. A Monte Carlo analy-

Transistor	Low monitor (W/L)
T_{p1}, T_{p2}	10/0.35
T_{l1}, T_{l2}	10/0.35
T_{eq}	10/0.35
T_{in1}	10/0.6
T_{in2}	5/0.6
T_b	25/0.35

Table 4.2: Channel width and length of the transistors of the low level monitor.

sis has been carried out also for the low level monitor and using the same tolerance parameters: 21% for the threshold voltage, 8% for the gate oxide thickness, 5% for the mobility and 5% for the channel widths and lengths. The simulation results shown in Fig. 4.5 are obtained with 35 Monte Carlo runs. These Monte Carlo runs were applied in each NW point in order to find the lower and upper curves. For the lower curve, it was taken the NH values that generated at least one detection in a given value of NW in one iteration

while in the other iterations the noise pulse was not detected. This operation has been made for each NW point of the lower curve. For the upper curve, the NH values, that generate the monitor detection in all iterations in a given value of NW, were taken. This process was repeated for each value of NW of the upper curve.

Because variations of the process parameter occur, the upper (lower) limit of the detectable (undetectable) region goes upward (downward). As a consequence, only those points located above (below) the upper (lower) curve can be assured as detectable (undetectable). The noise height (NH) is almost constant for long noise widths. The DC performance of the low level monitor could be considered as a case of the longest noise pulse width of the SUV. The minimum NH detected by the monitor in this case could be considered as the indicated by the typical curve on Fig. 4.5. The minimum NH detected by the low level monitor for the longest noise pulse width (100psec) in the typical case was 0.23V. This value could change by the action of process variations as it is shown in the upper and lower curves in Fig. 4.5. The regions can be modified by proper design of the channel transistor geometries of the monitor.

4.1.2 Module with controlled frequency of the SUV

The chip contains a module to verify signal integrity at different frequencies of the SUV (See Fig. 4.6). This module consists of several blocks (See. Fig. 4.7) The SUV is generated internally by a voltage controlled oscillator (VCO), which is controlled by external DC voltages (Vpc and Vnc). Using these voltages, signals at frequencies from 120MHz to 670MHz are obtained. The signals generated by this module can be seen externally. A frequency divider by 16 is used to divide the frequency of the signal generated by the VCO. The output of the frequency divider is sent out to an output pin. The module allows to generate undershoots and overshoots (noise pulses) in the SUV. One pin ($V\phi$) selects the generation of either the undershoot or the overshoot. The magnitude of these noise pulses is controlled externally by the DC voltages (Vn and Vp). The undershoots and overshoots in SUV are detected by the high and low level monitors respectively.

Both, the high and low level monitors are implemented in this module for sensing three signals. Each block is explained next.

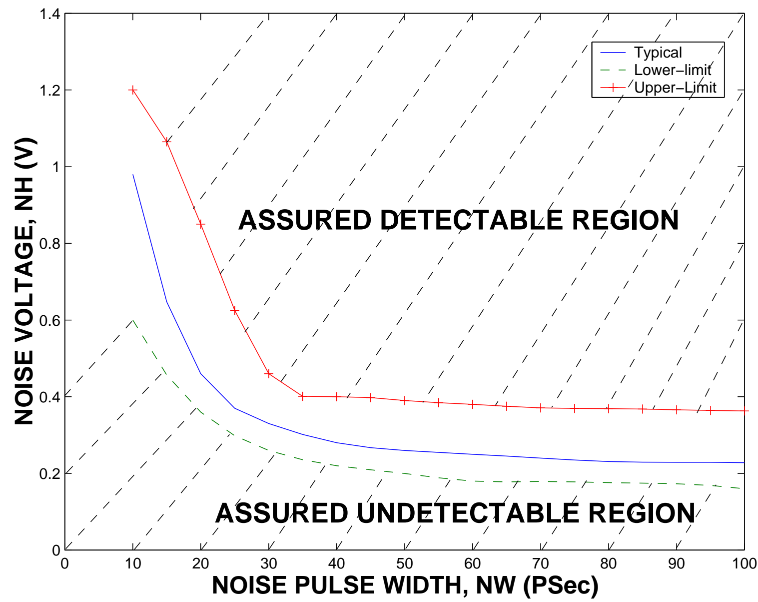


Figure 4.5: Pulse width duration of the noise (NW) versus voltage noise (NH) for the low level monitor where the assured detectable and undetectable region are shown. These regions were obtained by considering process variations.

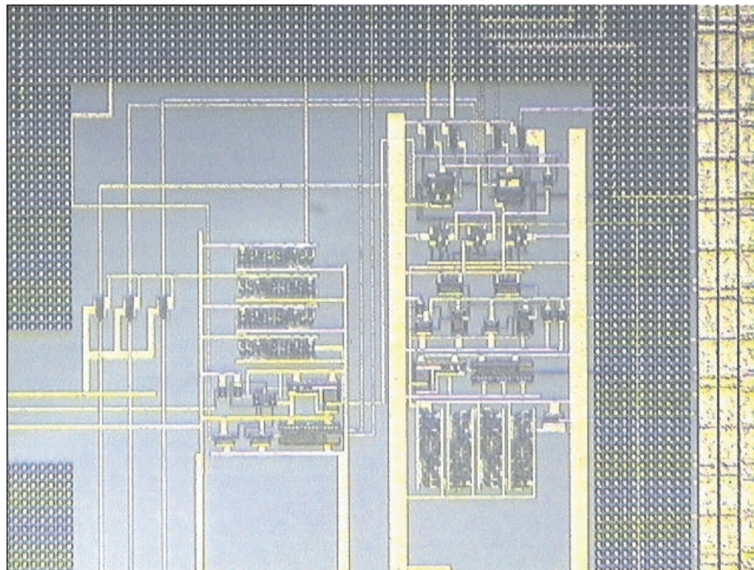


Figure 4.6: Picture of the module with controlled frequency of the SUV.

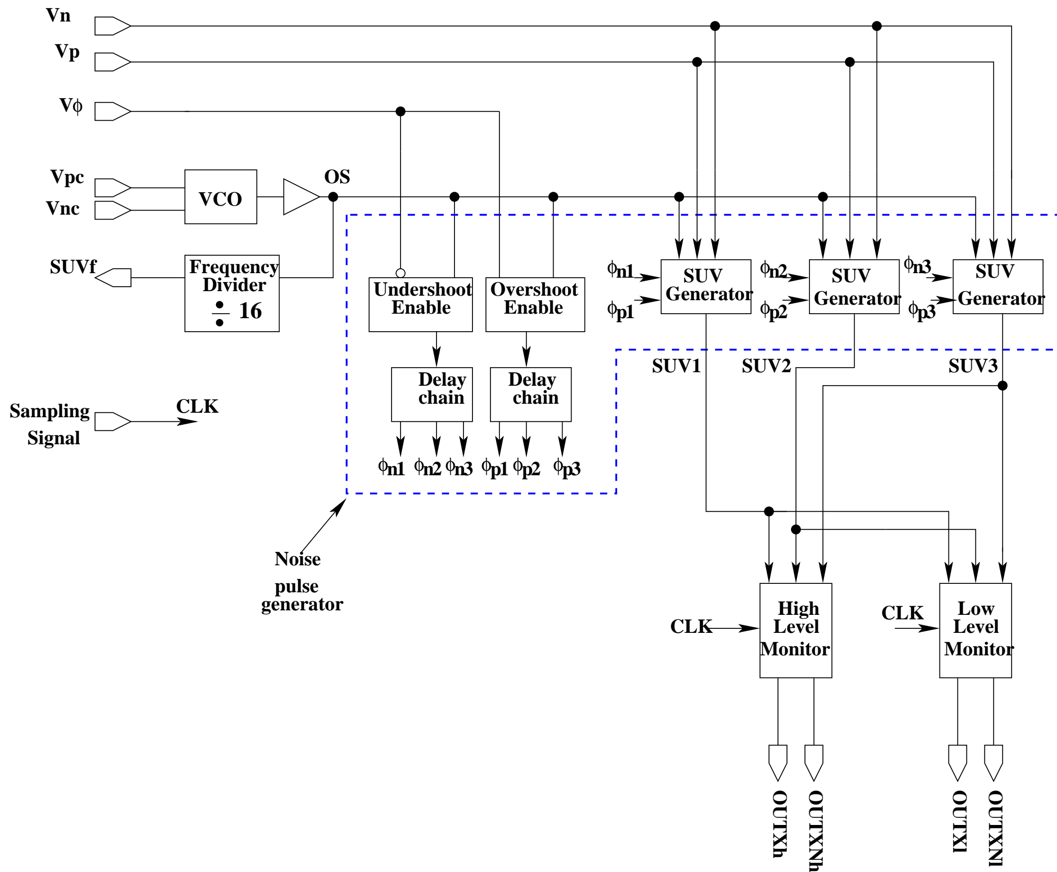


Figure 4.7: Block diagram of the module with controlled frequency of the SUV.

VCO

The VCO has been designed in order to generate internally the SUV. The VCO generates signal frequencies from $120MHz$ to $670MHz$. The VCO is implemented by a ring oscillator of three stages. The spread of frequencies are obtained by setting up the control voltages Vpc and Vnc. The control voltage change the (dis)charge current of the inverters. The schematic of the VCO implemented is shown in Fig. 4.8. The performance obtained for the

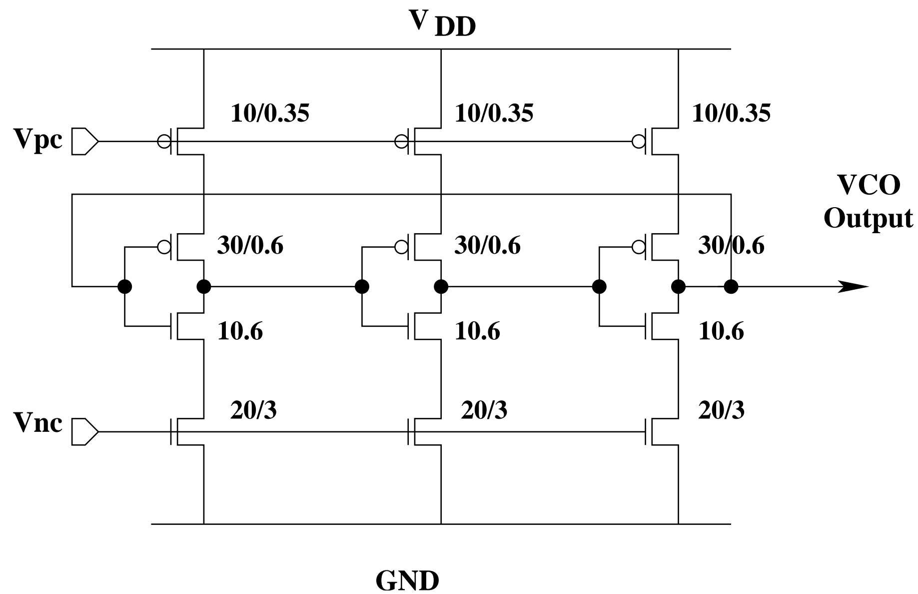


Figure 4.8: VCO implemented to generate the SUV. Two signals are used to control the VCO frequency.

fabricated VCO is close to the estimated by simulation. This characteristic is important because the noise pulse generator, the high and low level monitor and additional circuitry were designed into the VCO frequency range obtained by simulation. The simulated and experimental VCO frequency response to different Vnc control voltages is shown in Fig. 4.9. The control voltage Vpc is hold to 0 volts in this experiment.

Frequency Divider

The coherence relations between the sampling signal and the SUV have been obtained because, the frequency of the signal generated by the VCO is known.

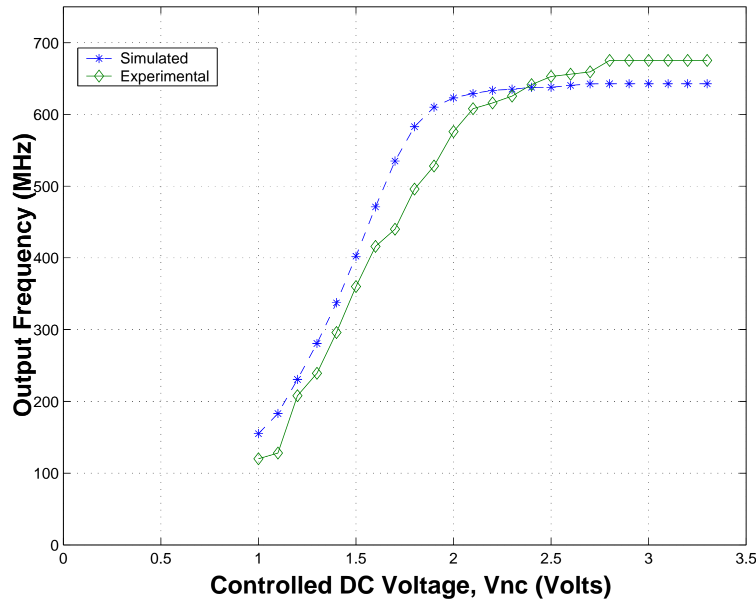


Figure 4.9: Simulated and experimental curves of the VCO frequency response to different values of Vnc.

The internal signal frequencies could be high (1.8GHz, for example) and these high frequency signals could be difficult to observe properly at the output pads. Because this, a frequency divider for the SUV signal has been implemented. The frequency divider allows to inspect at the output pin the signal frequency generated by the VCO. The frequency divider by 16 allows to see a low signal rate at the output pin. The schematic of the frequency divider is shown in Fig. 4.10a. It consists of an arrangement of four flip-flops. This arrangement divide the input frequency of the signal by 16. The transistor level diagram of each flip-flop is shown in Fig. 4.10b.

The performance of the frequency divider has been validated experimentally. Two measurements show the performance of the fabricated frequency divider. First it is shown the frequency division of a signal of 10MHz. Fig. 4.11 shows the input signal (Fsig) at 10MHz. This signal is generated externally by a function generator. The lower signal shows the output of the frequency divider (Fdiv). This signal has a frequency of 625KHz. The second measurement is shown in Fig. 4.12, the input signal (Fsig) has a frequency of 50MHz. The output of the frequency divider (Fdiv) shows a frequency

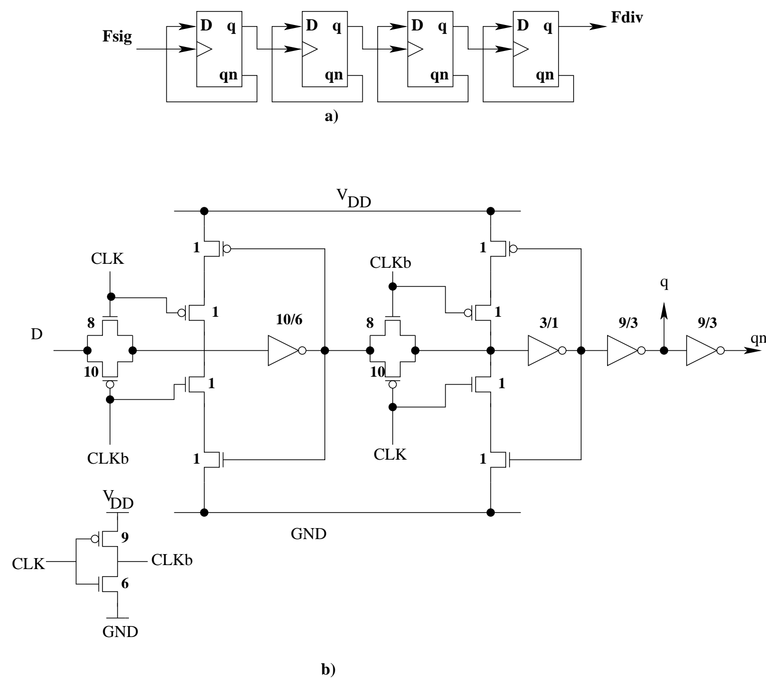


Figure 4.10: Frequency divider by 16: a) Flip-flops arrangement used to generate the frequency divide of the SUV, b) transistor level diagram of the implemented flip-flop.

of 3.12MHz. These measurements are only to show the frequency divider performance. The noise of the input signal has been ignored.

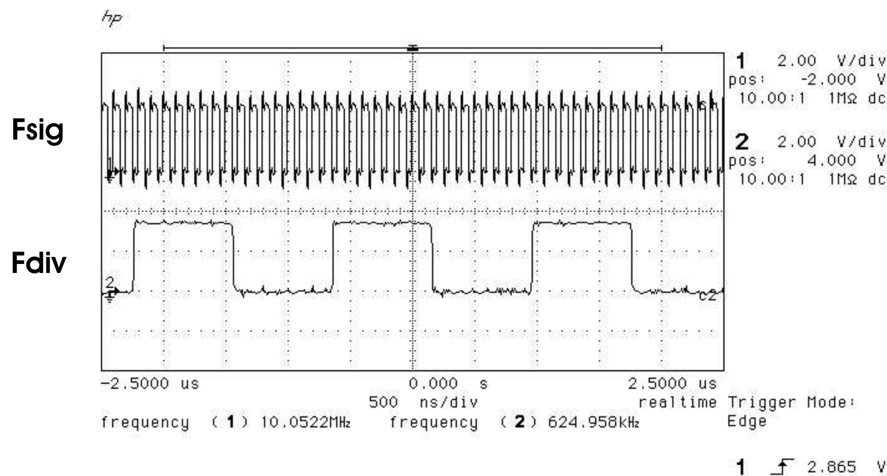


Figure 4.11: Example of the frequency divider performance when the input signal has a frequency of 10MHz.

Noise Pulse Generator

A noise stimuli is applied to the signal generated by the VCO to produce the SUV with integrity degradation. The noise pulse generator basically is composed of two circuits (See Fig. 4.7). A circuit to inject the noise stimuli to the SUV is needed. This circuit is called the SUV generator. The second circuit allows to generate two kind of noise stimuli, one to select undershoots and other to select overshoots in the SUV (See Fig. 4.7). The schematic of the SUV generator is shown in Fig. 4.13. The signal generated by the VCO is the input of the buffer B1. This buffer is needed to give enough strength to the SUV. The SUV obtained by this circuit goes to the high and low level monitors (See Fig. 4.13). The circuit generates overshoots if the transistor M1 is activated by the pulse ϕ_p. The undershoots are generated if the transistor M2 is activated by the pulse ϕ_n. The magnitude of the overshoots and the undershoots is controlled by the external signals Vp and Vn respectively. The overshoots must be generated only when the SUV is on the low logic

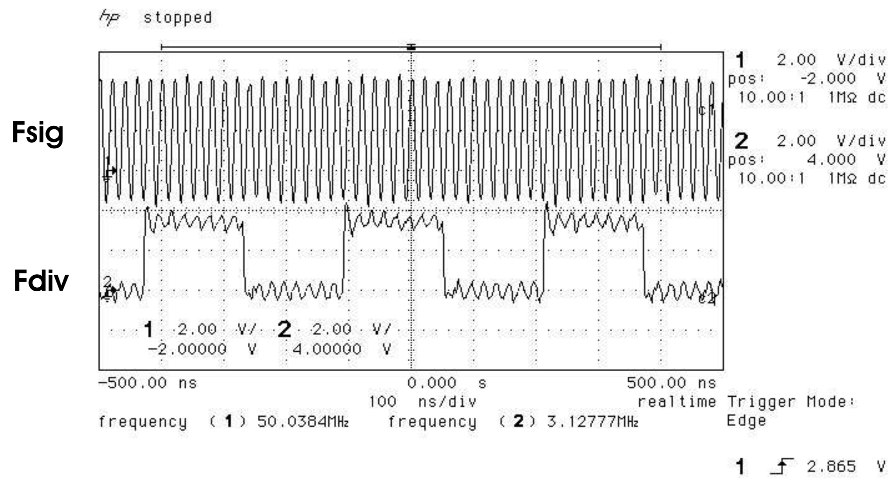


Figure 4.12: Example of the frequency divider performance when the input signal has a frequency of 50MHz.

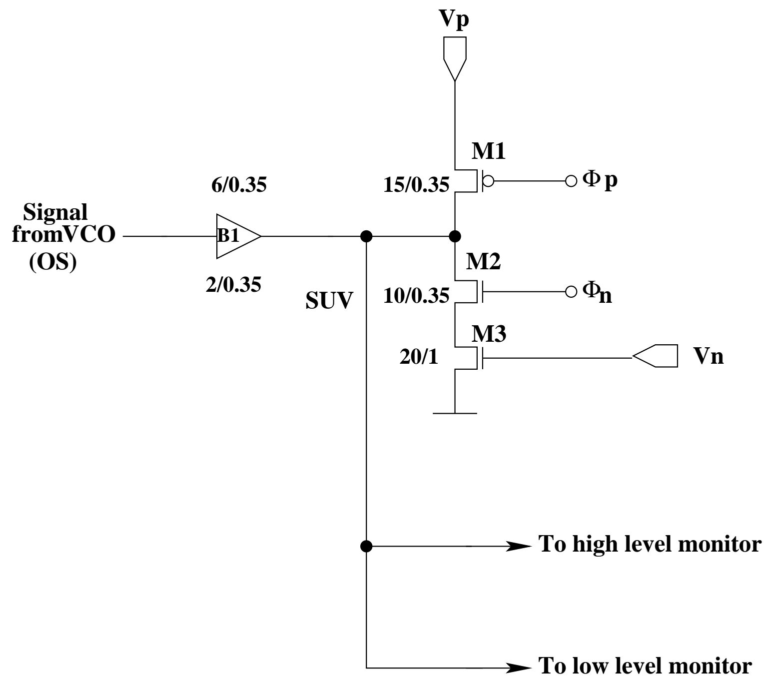


Figure 4.13: Schematic of the SUV generator.

level, and the undershoots must be generated when the SUV is on the high logic level. These issues are solved by generating the pulses ϕ_p and ϕ_n at the correct times. The pulses ϕ_p and ϕ_n are generated when the SUV goes from high to low and low to high. The circuit used to generate these pulses is shown in Fig. 4.14.

The signal generated by the VCO (OS) is input of two delay cells, one

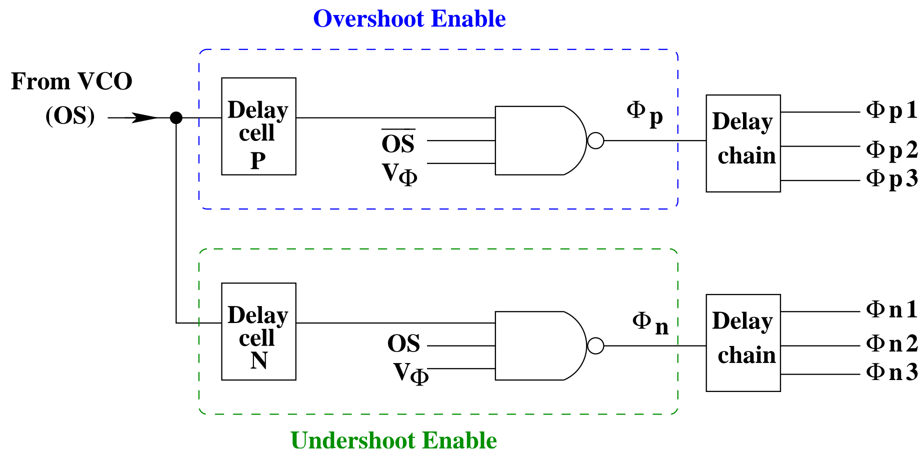


Figure 4.14: Schematic of the circuit used to generate the pulses ϕ_p and ϕ_n to inject the overshoots and undershoots to the SUV.

for the overshoot pulse generator and the other for the undershoot pulse generator. The output of the delay cell P (N) is one of the three inputs of the 3-input NAND gate. This NAND gate generates a pulse when $\overline{OS}$ (OS) has a transition from high (low) to low (high). $\overline{OS}$ (OS) is the other input of the 3-input NAND gate. It is possible to select what kind of pulse will be generated by the external signal $V\phi$. If $V\phi$ is high (low) the pulse ϕ_p (ϕ_n) will be generated.
In our prototype circuits, three signals are verified, hence three circuits to inject noise are needed, but only one overshoot and one undershoot pulse generators are required. The delay chain is used to move the location of the pulse generated ϕ_p (ϕ_n). The generation of three ϕ_p pulses at different locations is shown in Fig. 4.15. In this case the signal $V\phi$ is a high logic level. The upper panel shows the signal OS and the lower panel shows the ϕ_p pulses generated by the overshoot pulse generator. Fig. 4.16 shows the generation of three ϕ_n pulses. To accomplish this action the signal $V\phi$ must

be in a low logic level. The upper panel shows the signal OS and the lower panel depicts the locations of the three ϕ_n generated by the undershoot pulse generator. Fig. 4.17 depicts the action of applying one ϕ_p to the injected

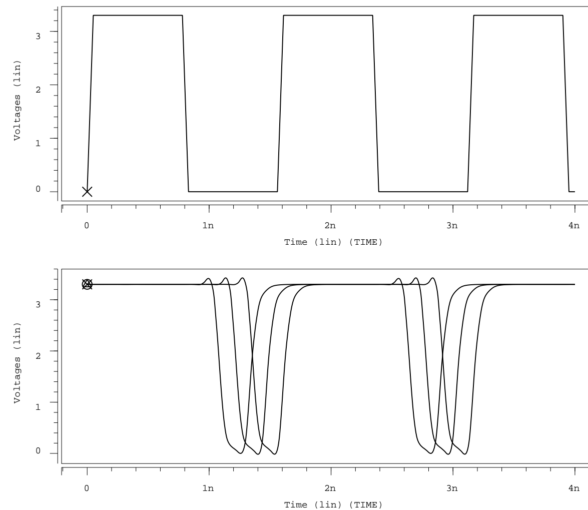


Figure 4.15: Simulation results of the overshoot pulse generator where three ϕ_p pulses have been produced.

noise circuit (See Fig. 4.13) for generating an overshoot at the low logic level of the SUV. The upper panel shows the ϕ_p pulse applied. The lower panel shows the SUV with a overshoot in its low logic level. The magnitude of the overshoot is controlled by the external DC voltage Vp. The maximum voltage value of the overshoot is when $VP = V_{DD}$. Fig. 4.18 shows the obtained SUV (lower panel) when the pulse ϕ_n (upper panel) is applied. The SUV presents an undershoot in its high logic level by the action of the pulse ϕ_n. The magnitude of the undershoot is controlled by the DC voltage Vn. The maximum undershoot voltage value is when $Vn = 3.3$

High and low level monitors

The module contains one high and low level monitors to verify the SUV for undershoots and overshoots respectively. The high level monitor has been designed to manage three SUVs. he schematic of the high level monitor implemented in this module is shown in Fig. 4.19. The low level monitor implemented in this module is able to verify also three SUVs. The schematic

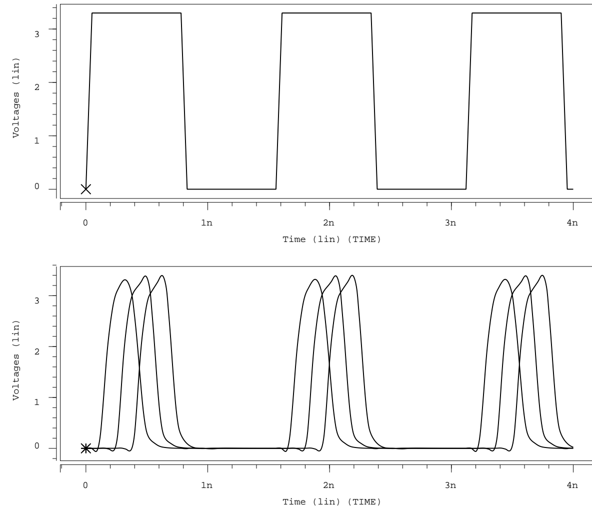


Figure 4.16: Simulation results showing the three ϕ_n pulse have been generated by the undershoot pulse generator.

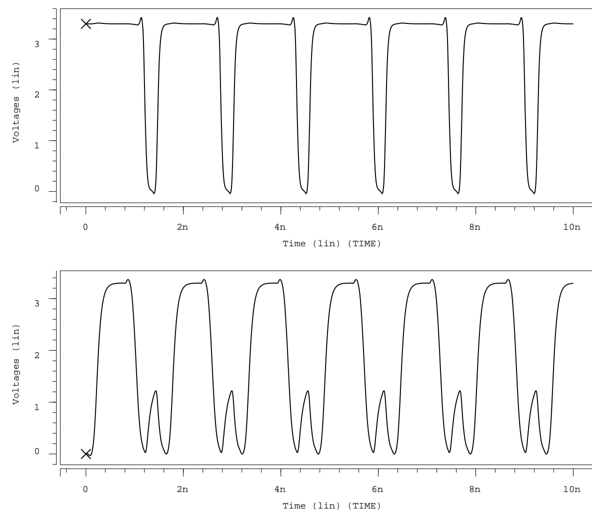


Figure 4.17: SUV with overshoot generated by the injected noise circuit.

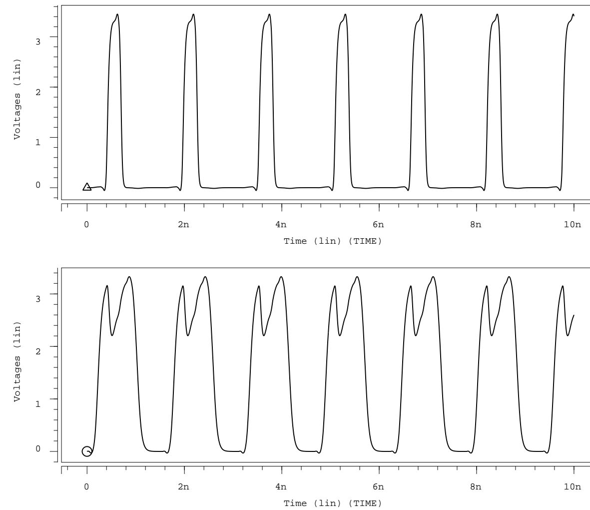


Figure 4.18: SUV with undershoot generated by the injected noise circuit.

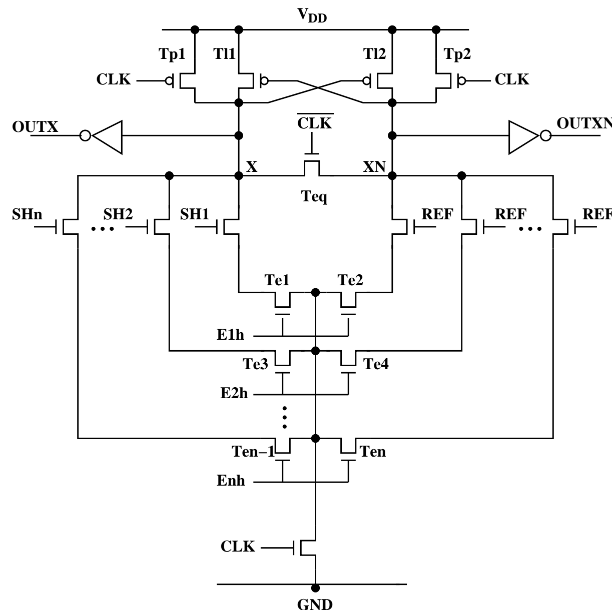


Figure 4.19: High level monitor implemented for the module with controlled frequency of SUV.

of this monitor is shown in Fig. 4.20 The transistor channel widths and

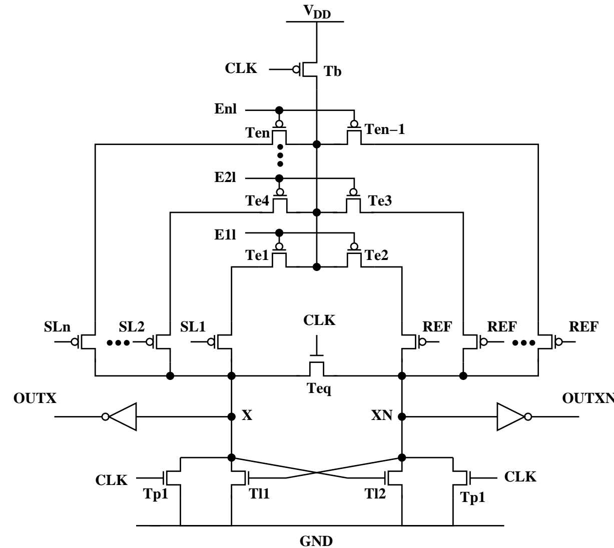


Figure 4.20: Low level monitor implemented for the module with controlled frequency of SUV.

lengths for the high and low level monitors implemented for the module with controlled frequency of the SUV are shown in the table 4.3.

4.1.3 Module with fixed high frequency of the SUV

The second module has been designed to generate a high frequency SUV. The block diagram of this module is shown in Fig. 4.21. In this module all the circuits explained above have been redesigned in order to operate at a higher frequency. Few modifications have been required to implement this module. The channel width of some transistors of this module are different than for the module explained above. Fig. 4.22 shows the picture of this module. The SUV in this module is also generated for a free running three stages ring oscillator. The maximum frequency obtained by this oscillator was of 1.8332GHz, but due to the experimental requirement to inject noise to the SUV generated, the circuit implemented to generate this noise limits the maximum frequency allowed of the SUV. This oscillator is controlled by the signal *Ctl* (See Fig. 4.21). The maximum frequency of the SUV achieved by this module was 917MHz. At this frequency we assure the SUV

Transistors	High monitor (W/L)	Low monitor (W/L)
T_{p1}, T_{p2}	10/0.35	10/0.35
T_{l1}, T_{l2}	25/0.35	10/0.35
T_{eq}	10/0.35	10/0.35
T_{in1}	10/1	10/1
T_{in2}	5/1	5/1
T_{e1} to T_{e6}	8/0.35	10/0.35
T_b	15/0.35	25/0.35

Table 4.3: Channel width and length of the transistors of the high and low level monitors.

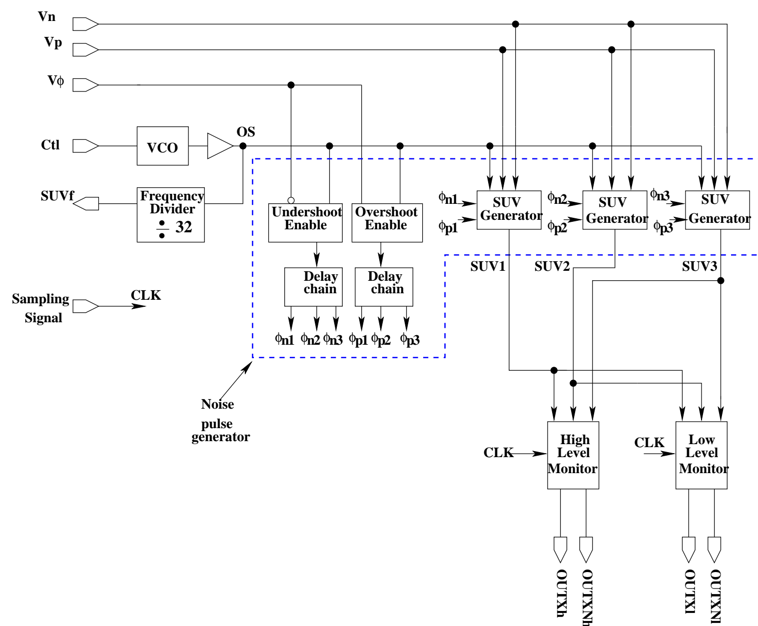


Figure 4.21: Block diagram of the module with high fixed frequency of SUV. Transistors of some circuits have been resized in order to obtain high speed performance. The VCO is just controlled by the signal Ctl.

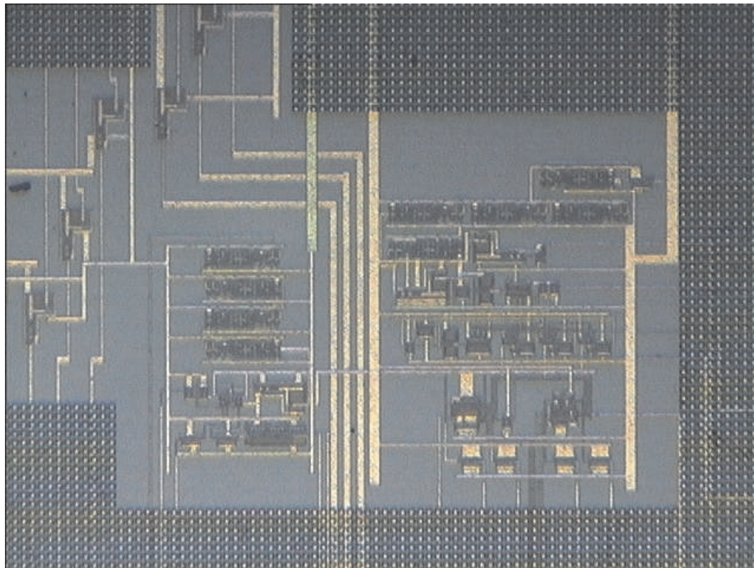


Figure 4.22: Picture of the module implementing high frequency signals generation

generation with proper overshoots and undershoots. The circuitry designed to generate the overshoots and the undershoot receives the signal frequency of the oscillator divided by two (917MHz).

4.2 Measurements for the high level monitors

The undershoots generated in the SUV are verified by the high level monitor. First the DC performance of the high level monitor is presented. Next, the dynamic performance of the monitor is shown for the noise-free and with noise cases of the SUV at frequencies of the SUV. A full set of measurement results is presented for a frequency of 640MHz of the SUV. Then, results for a higher frequency (917MHz) of the SUV are presented. During all the measurements, only one SUV is enabled while the other two remain inactive. Different magnitude of the undershoot voltage have been considered in all cases. The main goals of theses experiments shown in this section are:

- to observe the monitor output for the case of signal integrity violation by applying different DC voltages in the monitor input

- to obtain the dynamic behavior of the monitor at frequency of 640MHz and 917MHz
- to get the monitor response at two different sampling rates for the cases of signals with or not integrity violations.

The goal for DC performance was achieved by using the individual high level monitor. An arbitrary sampling signal was applied in order to obtain the monitor output. Because the monitor input signal is a DC voltage for this case, any sampling frequency will produce the same results. The DC input voltage was modified by small steps from VDD to the voltage that produces no pulses in the monitor output. No pulses in the monitor output means the detection of signal integrity violation. The dynamic behavior was obtained by the module with controlled frequency of the SUV for the dynamic performance at 640MHz, and the module of the high frequency for the monitor dynamic performance at 917MHz. Two coherent sampling were applied for the monitor for obtain the monitor output for the cases of the signals with or not integrity violation.

4.2.1 Measurements in DC

In order to evaluate the DC performance of the proposed high level monitor, a DC voltage at its input is applied. This voltage is decreased until a change at the monitor outputs is observed, which indicates that it is the minimum detectable DC noise voltage. For the case of noise-free SUV the input voltage level must be VDD (3.3V for our case) and at each sampling signal evaluation (CLK=High) the node $OUTX$ must commute. Fig. 4.23 shows this behavior. For the case of the signal integrity violation, the DC input voltage is decreased. The voltage level at which the monitor output $OUTX$ remains to a low logic level is 2.32V (See Fig. 4.24). It means that a noise pulse of voltage magnitude equal or greater than 980mV will be detected by the monitor. This result is close to the one predicted by the simulated monitor performance curve shown in Fig. 4.3. The magnitude of 980mV is close to the value obtained in the performance curve (See Fig. 4.3) for the longest noise pulse width of 700ps.

The same measurements have been made for different chips in order to observe the process variation impact on the minimum detectable noise voltage value of the high level monitor in different chips. Fig. 4.25 Shows the values

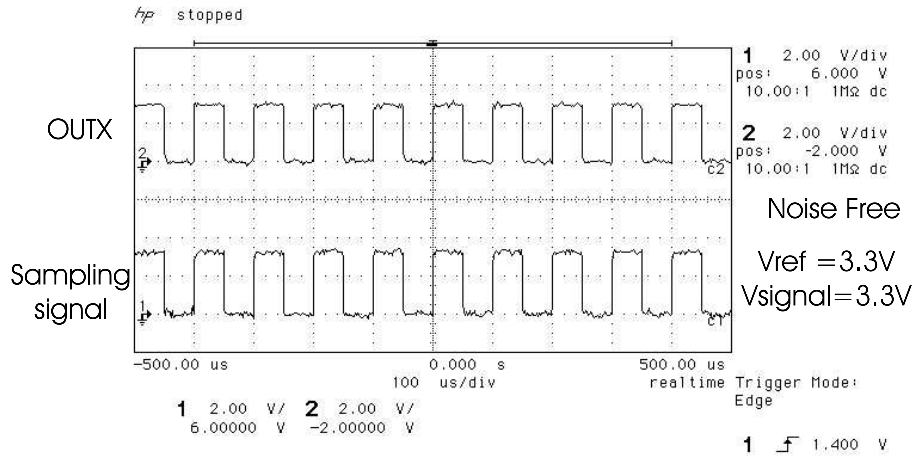


Figure 4.23: Output of the high level monitor when the SUV is a DC voltage level of 3.3V. Signal integrity violation does not occurs.

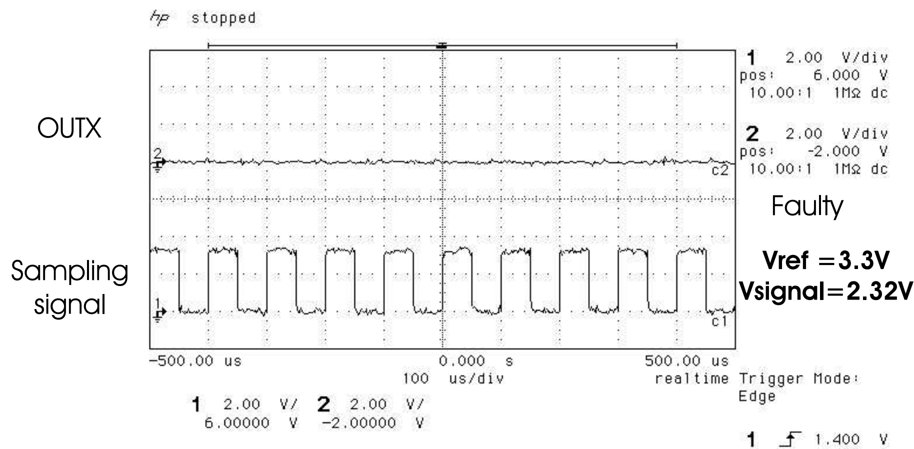


Figure 4.24: Output of the high level monitor when the SUV is a DC voltage level of 2.32V. Signal integrity violation occurs.

obtained. The minimum detectable NH value achieved by the high level monitor is 980mV and the maximum is 1.03V.

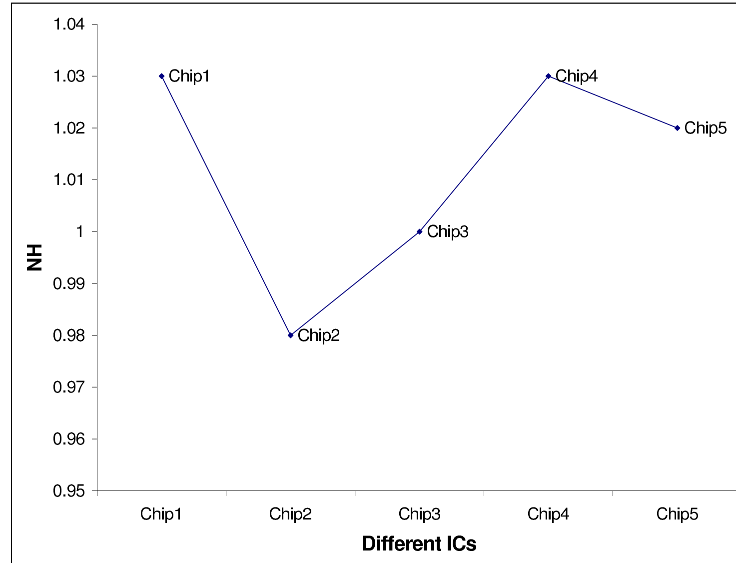


Figure 4.25: Minimum detectable noise voltage obtained for the same circuit in different chips.

4.2.2 Measurements for the module with controlled frequency of the SUV, $f_{SUV} = 640MHz$

The main propose of these measurements is to obtain the dynamic behavior of the high level monitor at 640MHz. To accomplish this, the following is made:

- The internal VCO for the module with controlled SUV frequency is set to 640MHz.
- Two coherent sampling frequency (frequency 1 and 2) are found in order to obtain 8 and 12 samples in one unit test period (UTP). Four and six samples are taken in the low and high logic level of the SUV for frequency 1 and 2 respectively.
- No external stimuli is applied in order to generate the noise-free SUV at 640MHz.

- Applying frequency 1 and 2, the monitor outputs $OUTX$ and $OUTXN$ are observed
- External stimuli is applied in order to produce undershoots at the high level of the SUV. These undershoots have enough magnitude to produce signal integrity violations.
- Applying sampling frequency 1 and 2, we inspect the monitor outputs $OUTX$ and $OUTXN$

The goal is to observe the signals in the monitor outputs when the SUV is free or with noise (undershoots) and to identify when a signal integrity violation has occurred. The measurements of the dynamic performance for the high level monitor at a frequency of 640MHz of the SUV are presented. The following measurements are made:

1. Noise free at coherence frequency 1, fclk=8.88MHz
2. Noise free at coherence frequency 2, fclk=13.3MHz
3. With noise pulse at coherence frequency 1, fclk=8.88MHz
4. With noise pulse at coherence frequency 2, fclk=13.3MHz
5. With noise pulse at coherence frequency 1, noise pulse 2
6. With noise pulse at coherence frequency 1, noise pulse 3

The first two show the dynamic performance of the high level monitor for two different coherent relations chosen for the sampling frequency. The next two show the behavior under a noise pulse for the two previously chosen coherent relations. The used noise pulse estimated from simulations has a height (NH) of 1.1 Volts and a width (NW) of 410ps. In the measurement results 5 and 6, the noise pulse is modified. The coherence frequency 1 is used. Fig. 4.26 shows the shape of the noise pulse obtained by simulation.

Let's explain the expected results before showing the measurement results. The response of the high level monitor depends on the sampling frequency (See chapter 3). When the SUV has not integrity violation its outputs behavior is as follows: The node $OUTX$ remains in a low logic state, while the SUV is sampled in the low logic state. When SUV is sampled in a high

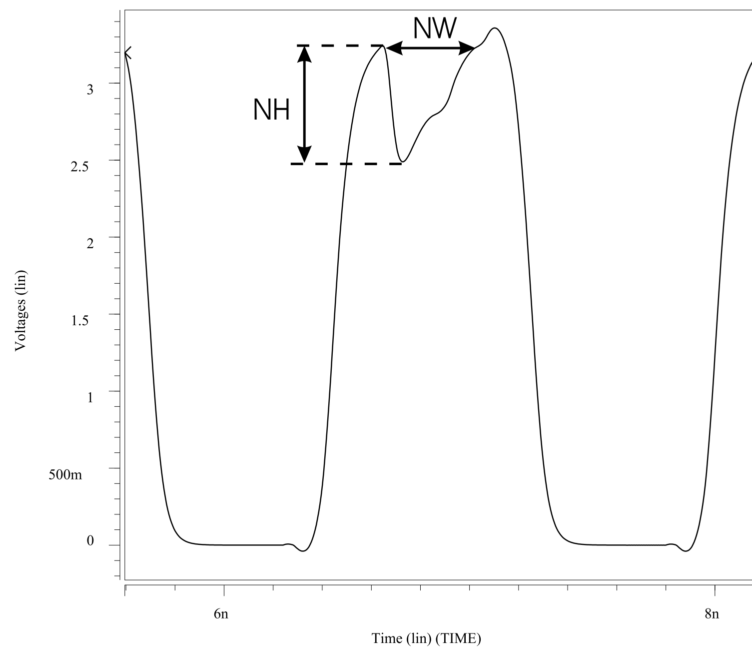


Figure 4.26: Shape of the noise pulse injected in the SUV in its high logic level

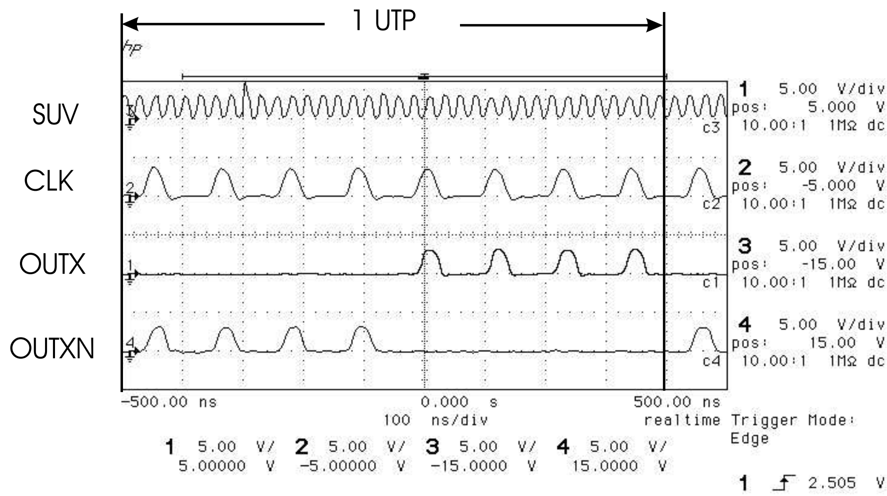


Figure 4.27: Output of the high level monitor when the SUV is free of noise and 8 samples are taken to the SUV in one UTP, $f_{SUV} = 640MHz$, $f_{CLK} = 8.88MHz$.

logic state the node $OUTX$ commutes from low to high logic state when the SUV has not a signal integrity violation. Otherwise $OUTX$ remains at a low logic level at the sampled point. Fig. 4.27 shows the measurement made to the high level monitor when the SUV is free of noise and 8 samples are taken (measurement 1).

The signal SUV shown in Fig. 4.27 is the internal generated SUV divided by 16, internally the SUV has a frequency of 640MHz. The next signal (CLK) is the sampling signal, here it is important to note that due to coherent sampling inside of the UTP just 8 samples of the SUV have been taken. The sampling frequency is 8.88MHz. The next signal shows the signal at node $OUTX$. During the first 4 samples this node remains at a 0 logic indicating that the SUV is sampled in the low logic state. For the last 4 samples, the node $OUTX$ presents pulses indicating that the SUV is sampled in the high logic state. Because the SUV is noise-free the last 4 samples produce that the node $OUTX$ commute 4 times. The last panel shows the signal in the node $OUTXN$ which has a complementary behavior of the node OUT for this case.

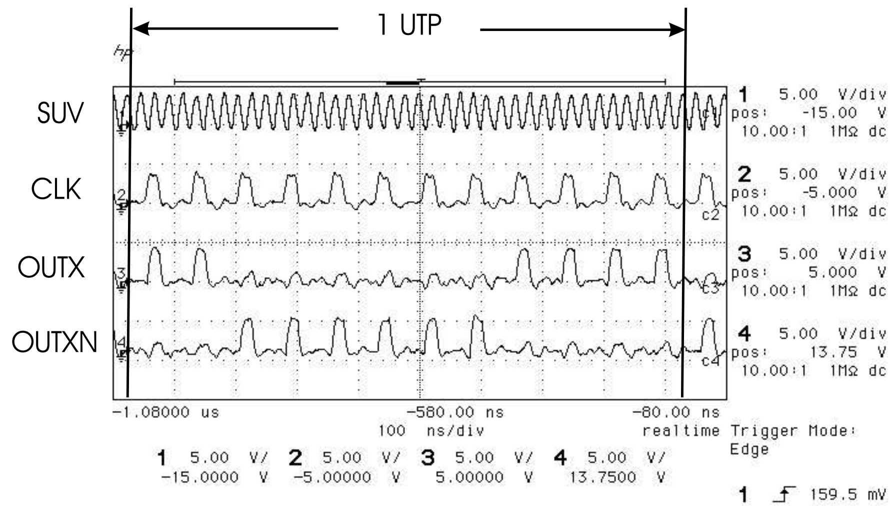


Figure 4.28: Output of the high level monitor when the SUV are free of noise and 12 samples are taken to the SUV in one UTP, $f_{SUV} = 640MHz$, $f_{CLK} = 13.3MHz$

For the measurement 2, the number of samples taken to the SUV are increased, hence the coherent sampling is changed. A sampling frequency of 13.3 MHz is required for taken 12 samples to the SUV. The case for the noise-free SUV is shown in Fig. 4.28. From the upper to lower signals are shown SUV, CLK, OUTX, and OUTXN respectively. From left to right into the UTP, two samples are taken in the high logic level of SUV and the node $OUTX$ presents pulses in these 2 samples. In the next six samples the SUV is sampled in the low logic level hence, the node $OUTX$ remains in logic 0. In the last four samples the SUV is again sampled in the high logic level. Because the SUV is noise-free, all samples in the high logic level of SUV produce pulses in the node $OUTX$. It is important to note that six samples are taken in the high and six in the low logic levels of the SUV.

When a noise pulse is injected to the SUV, it will be detected by a missing pulse when the SUV is sampled at the high logic state. The results of the measurement 3 are shown in Fig. 4.29. The values of NH and NW have been obtained by electrical simulation. The undershoot in the SUV is generated by the noise pulse generator. The magnitude of the undershoot is controlled by the external DC signal Vn that in this case is 1.5V. The upper signal

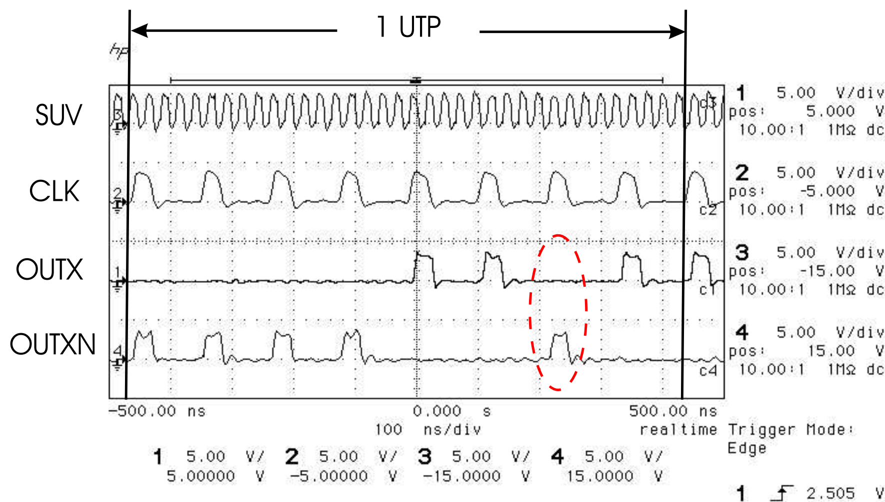


Figure 4.29: Output of the high level monitor for the SUV with noise and 8 samples are taken to the SUV in one UTP, $f_{SUV} = 640MHz$, $f_{CLK} = 8.88MHz$, NH=1.1V, NW=410ps.

shows the SUV divided in frequency by 16, the next signal (CLK) is the sampling frequency, with this sampling frequency 8 samples are taken to the SUV. Next signal ($OUTX$) shows the behavior of the node $OUTX$. In the first 4 samples of SUV the node $OUTX$ remains to 0 as the case of the noise-free SUV because the SUV is sampled in the low logic level. When the SUV (with integrity degradation) is sampled in a high logic state occurs a signal integrity violation which is detected by the monitor. It can be seen in the third sample of the SUV in the high logic level (seventh into the UTP) that the node $OUTX$ remains to a 0 and the node $OUTXN$ (lower panel) commute from low to high. In the two next sampling periods the node $OUTX$ commute and the node $OUTXN$ remains at a 0 logic.

The measurement 4 (See Fig. 4.30) has been made for the same noise pulse conditions. The number of samples taken to the SUV are 12 for this measurement. From the upper to lower signals are shown the signals SUV, CLK, $OUTX$, and $OUTXN$ respectively. From left to right into the UTP, the first sample taken into the UTP is in the low level of the SUV, in this sample the node $OUTX$ is a logic 0 and the node $OUTXN$ presents a pulse. In the next six samples the SUV is sampled in the high logic level, in the sec-

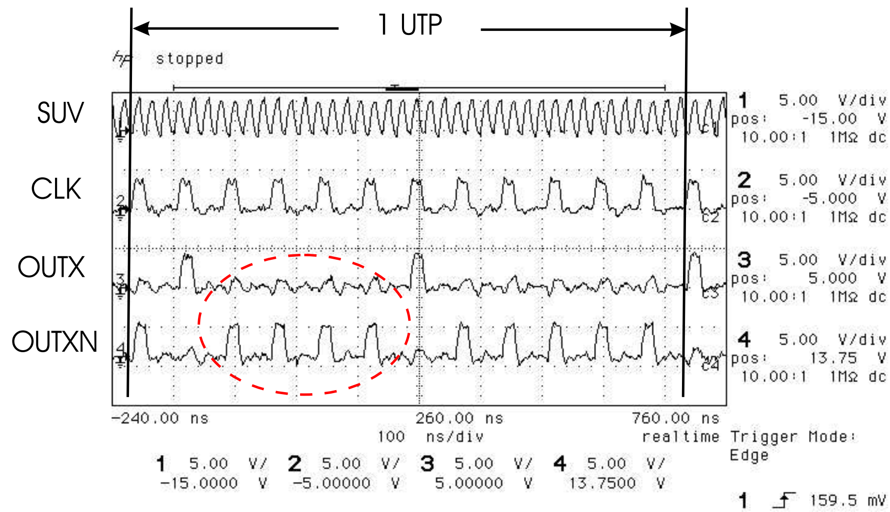


Figure 4.30: Output of the high level monitor when the SUV has a noise pulse and 12 samples are taken into the UTP, $f_{SUV} = 640MHz$, $f_{CLK} = 13.3MHz$, NH=1.1V, NW=410ps.

ond sample, the monitor sees a high logic level and the node $OUTX$ presents pulses. The monitor detects the integrity violation (undershoot) at the next four samples (samples from third to sixth in the UTP). In these samples the node $OUTX$ keeps in a logic 0 and the node $OUTXN$ presents pulses. This performance of the monitor outputs indicates the detection of the non allowed undershoot in the SUV. In the last five samples into the UTP the SUV are sampled in the low logic level, in this samples $OUTX$ remains in a logic 0 and $OUTXN$ presents pulses.

Figs. 4.31 and 4.32 show the high level monitor response for the case when the magnitude of the noise pulse is increased. This corresponds to the measurement 5 and 6. Note that in Fig. 4.31 two detections are obtained while Fig. 4.29 (same coherence relation) only one detection is achieved. In Fig. 4.32 the noise is increased even more. Three detections are achieved in this case. In these cases, 8 samples are taken into the UTP therefore the applied sampling frequency is 8.88MHz.

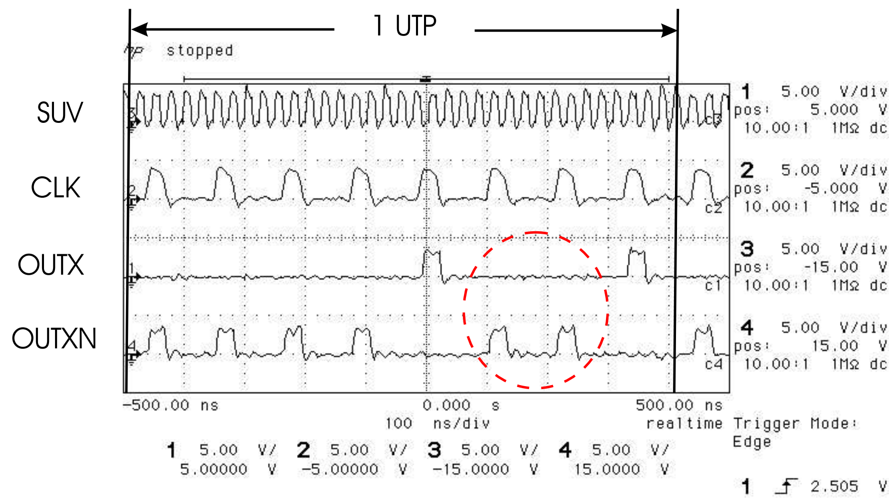


Figure 4.31: Output of the high level monitor when the SUV has a noise pulse. Two detection were obtained. 8 samples are taken into the UTP, $f_{SUV} = 640MHz$, $f_{CLK} = 8.88MHz$, NH=2V, NW=442ps.

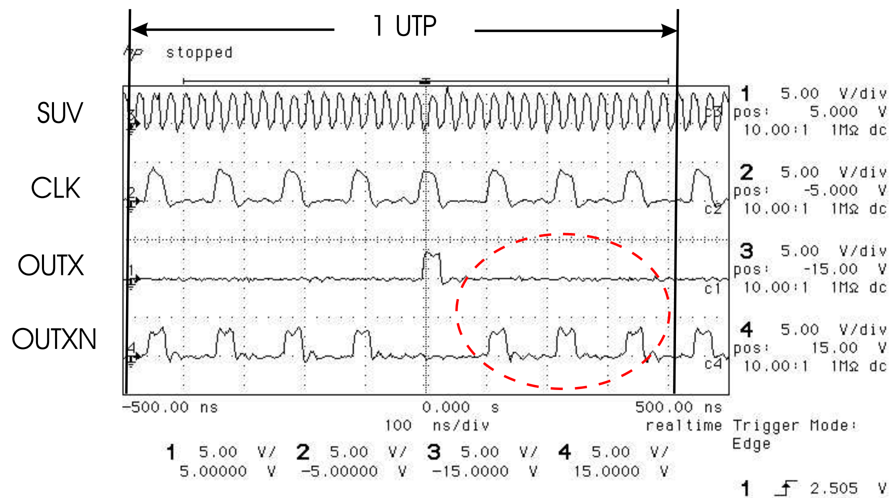


Figure 4.32: Output of the high level monitor when the SUV has a noise pulse. Three detection were obtained. 8 samples are taken into the UTP, $f_{SUV} = 640MHz$, $f_{CLK} = 8.88MHz$, NH=2.5V, NW=460ps.

4.2.3 Measurement to the module of the high frequency of the SUV, $f_{SUV} = 917MHz$

The propose of these measurements is to obtain the dynamic behavior of the high level monitor at 917MHz. The following is made to accomplish this:

- The internal VCO for the module of the high frequency of the SUV frequency is activated.
- Two coherent sampling frequency (frequency 1 and 2) are found in order to obtain 8 and 12 samples in one unit test period (UTP). Four and six samples are taken in the low and high logic level of the SUV for frequency 1 and 2 respectively.
- No external stimuli is applied in order to generate the noise-free SUV at 917MHz.
- Applying frequency 1 and 2, the monitor outputs $OUTX$ and $OUTXN$ are observed
- External stimuli is applied in order to produce undershoots at the high level of the SUV. These undershoots have enough magnitude to produce signal integrity violations.
- Applying sampling frequency 1 and 2, we inspect the monitor outputs $OUTX$ and $OUTXN$

The goal is to observe the signals in the monitor outputs when the SUV is free or with noise (undershoots) and to identify when a signal integrity violation has occurred.
Four measurement results are presented:

1. Noise-free at coherence frequency 1, fclk=6.8MHz
2. Noise-free at coherence frequency 2, fclk=13.6MHz
3. With noise pulse at coherence frequency 1, fclk=6.8MHz
4. With noise pulse at coherence frequency 2, fclk=13.6MHz

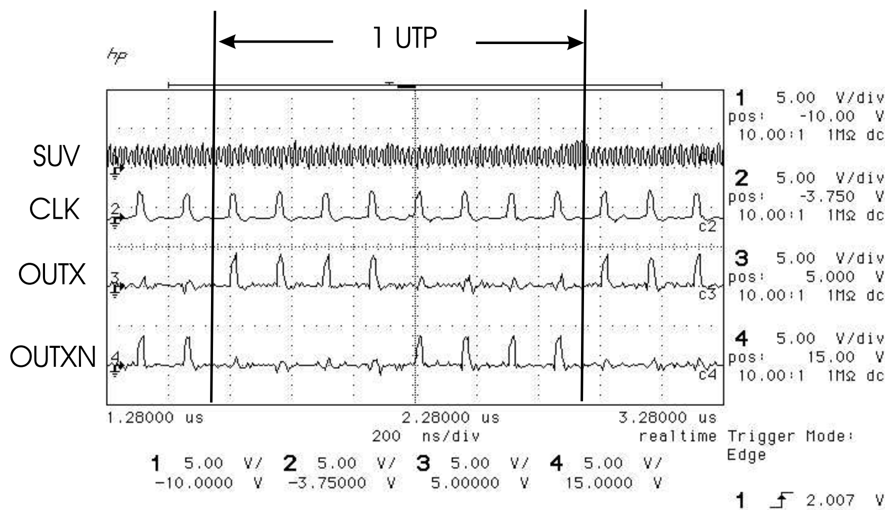


Figure 4.33: Measurement of the high level monitor response in the case of the noise-free SUV. 8 samples are taken into the UTP at rate of $f_{SUV} = 917MHz$, $f_{CLK} = 6.8MHz$.

The first two measurements made for the noise-free SUV show the dynamic performance of the high level monitor for two different coherent relations chosen for the sampling frequency. The next two show the behavior under a noise pulse for the two previously chosen coherent relations. The used noise pulse estimated from simulations has a height (NH) of 1 Volts and a width (NW) of 198ps.

Fig. 4.33 shows the measurement 1 results for the case of the noise-free SUV where 8 samples are taken into the UTP. In the first 4 samples from left to right the SUV is sampled in its high logic level and because the SUV is noise-free, $OUTX$ presents pulses on each CLK period and $OUTXN$ remains to a logic 0. In the last 4 samples the SUV is sampled in its low logic level, in these samples $OUTX$ is a logic 0 and $OUTX$ presents pulses.

Fig. 4.34 shows the measurement 2 results for the case of the noise-free SUV when 12 samples are taken into the UTP. The sampling frequency is 13.6MHz. From left to right, the first six samples are taken in the low logic level of the SUV, hence the node $OUTX$ remains in logic 0 and the node $OUTXN$ presents pulses. In the last six samples the noise-free SUV is

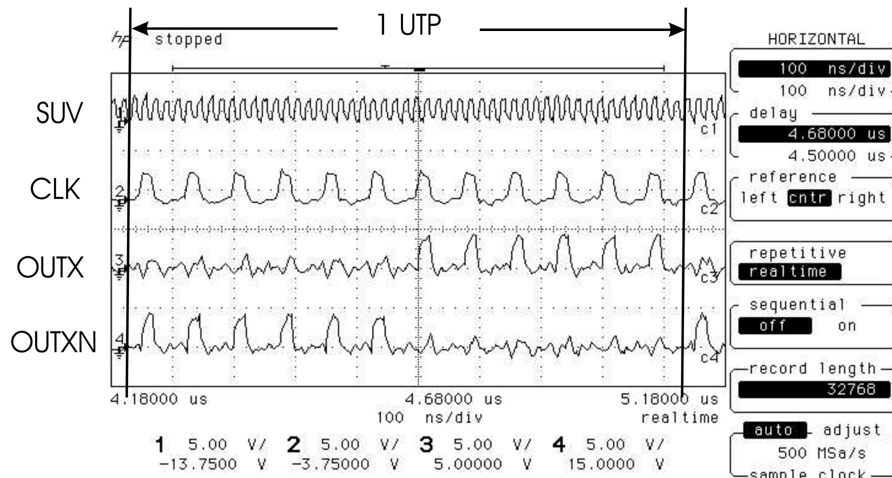


Figure 4.34: Measurement of the high level monitor response in the case of noise-free SUV. 12 samples are taken into the UTP, $f_{SUV} = 917MHz$, $f_{CLK} = 13.6MHz$.

sampled at its high logic level, hence $OUTX$ presents pulses indicating that there is not integrity violation of the SUV.

For the case of the SUV with noise an undershoot has been generated by the noise pulse generator in the high logic level of the SUV. Two coherent relations have been also used to validate the performance of the high level monitor for this case. Fig. 4.35 shows the measurement 3 results for the case of the verification of the SUV when 8 samples are taken into the UTP. From left to right, the first 4 samples are taken in the low level of the SUV with noise, hence $OUTX$ remains to a logic 0 and $OUTXN$ present pulses. In the last 4 samples the SUV is sampled at its high logic level. In the seventh sample into the UTP the high level monitor detects an integrity violation. The node $OUTX$ is a logic 0 and the node $OUTXN$ presents a pulse.

Fig. 4.36 shows the measurement 4 results for the case of SUV with noise when 12 samples are taken into the UTP. The sampling frequency is 13.6MHz. From left to right, in the first six samples the SUV is sampled in the low logic level, hence $OUTX$ remains to a logic 0 and $OUTXN$ presents pulses. In the next six samples the SUV is sampled in the high logic level.

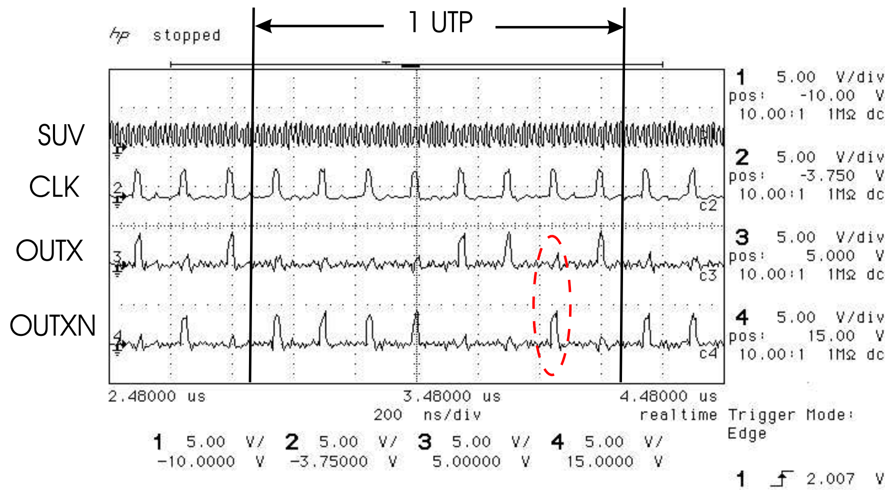


Figure 4.35: Measurement of the high level monitor response in the case of the SUV with signal integrity degradation. 8 samples are taken into the UTP, $f_{SUV} = 917MHz$, $f_{CLK} = 6.8MHz$, NH=1V, NW=198ps.

In the eleventh sample the undershoot is detected. $OUTX$ is a logic 0 and $OUTXN$ presents a pulse. In the other samples in which the SUV is sampled in the high logic level, $OUTX$ presents pulses.

The measurements presented in this section show the DC and dynamic behavior of the high level monitor. With DC behavior, the detectable voltage level for the fabricated high level monitor is found. Applying two different sampling frequencies, the monitor verify signals at 640MHz and 917MHz. For the sampling frequency 1 and 2, 8 samples were taken for SUV at 640MHz and 917MHz. If the SUV is noise-free, the node $OUTX$ presents 4 and 6 pulses when the SUV is sampled in the high logic level and $OUTXN$ presents no pulses for frequency 1 and 2 respectively. When the SUV is sampled in the low logic level, node $OUTX$ presents no pulses and node $OUTXN$ presents 4 and 6 pulses for frequency 1 and 2 respectively. If the SUV presents undershoots which generates integrity violations and the sampling frequencies 1 and 2 are applied, node $OUTX$ presents less than 4 or 6 pulses when the SUV is sampled in the high logic level for the sampling frequency 1 and 2 respectively. We conclude that a missing pulse or pulses when the SUV is sampled the high logic level indicates a signal integrity

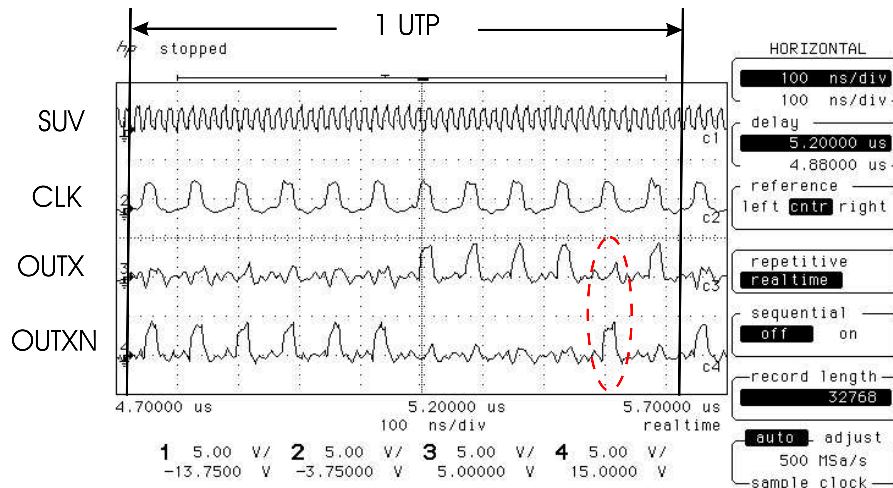


Figure 4.36: Measurement of the high level monitor response in the case of SUV with signal integrity degradation. 12 samples are taken into the UTP, $f_{SUV} = 917MHz$, $f_{CLK} = 13.6MHz$, NH=1V, NW=198ps.

violation. The number of missing pulse is increased when the magnitude and duration of the undershoot is increased.

4.3 Measurements for the low level monitors

In this section, measurements in low level monitor are presented. First the DC performance of the low level monitor is presented. Next, the dynamic performance of the monitor is shown for the noise-free and with noise cases of the SUV at frequencies of 640MHz, and 917MHz.

The main goal of this section are:

- to observe the low level monitor output for the case of signal integrity violation by applying different DC voltages in the monitor input
- to obtain the dynamic behavior of the low level monitor at frequency of 640MHz and 917MHz
- to get the low level monitor response at two different sampling rates for the cases of signals with or not integrity violations.

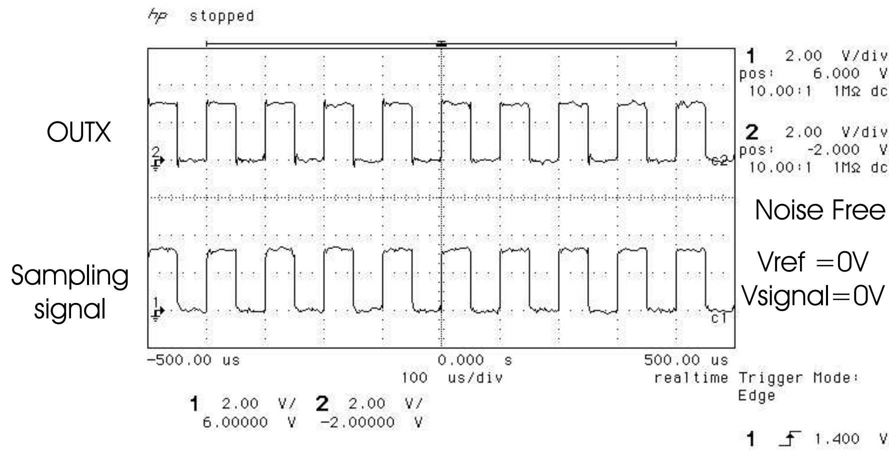


Figure 4.37: Output of the low level monitor when the SUV is a DC voltage level of 0V.

The goal for DC performance was achieved by using the individual low level monitor. Because the monitor input signal is a DC voltage for this case, any sampling frequency will produce the same results. The DC input voltage was applied from GND to the voltage that produces no pulses in the monitor output. No pulses in the monitor output means the detection of signal integrity violation. The dynamic behavior was obtained by the module with controlled frequency of the SUV at 640MHz, and the module of the high frequency with SUV at 917MHz. Two coherent sampling were applied for the monitor for obtain the monitor output for the cases of the signals with or not integrity violation.

4.3.1 Measurements in DC

To evaluate the DC performance of the proposed low level monitor, a DC voltage is applied at its input. This DC voltage is increased from 0 to a specific value until to observed a change at the monitor outputs. This indicates that the monitor has detected that voltage level. For the case of noise-free SUV the applied input voltage level was 0V and on each sampling signal the node $OUTX$ also commutes. Fig. 4.37 shows this behavior. For the case of the signal integrity violation, the DC input voltage is increased. The minimum detectable DC voltage is 0.65V (See Fig. 4.38). In this case the

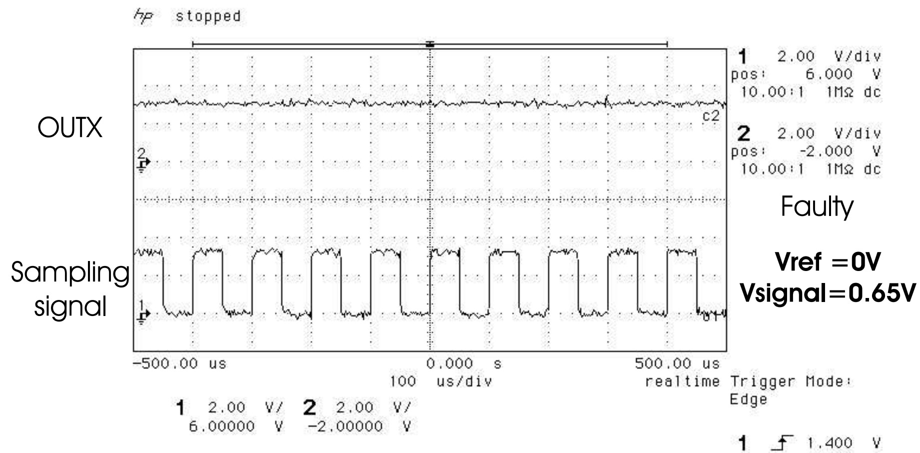


Figure 4.38: Output of the low level monitor when the SUV is a DC voltage level of 0.65V.

monitor output $OUTX$ remains to a high logic level. This result is close to the one predicted by the simulated monitor performance curve shown in Fig. 4.5. The magnitude of 650mV is close to the value obtained in the performance curve for the longest noise pulse width of 700ps. In order to observe the process variations impact on on the minimum detectable NH value by the low level monitor several measurements have been made to the low level monitor in different chips. Fig. 4.39 Shows the values obtained.

4.3.2 Measurements to the module with controlled frequency of the SUV, $f_{SUV} = 640MHz$

The goal of these measurements is to obtain the dynamic behavior of the low level monitor when it verify signals at 640MHz. To accomplish this, the following is made:

- The internal VCO for the module with controlled SUV frequency is set to 640MHz.
- Two coherent sampling frequency (frequency 1 and 2) are found in order to obtain 8 and 12 samples in one unit test period (UTP). Four and six samples are taken in the low and high logic level of the SUV for frequency 1 and 2 respectively.

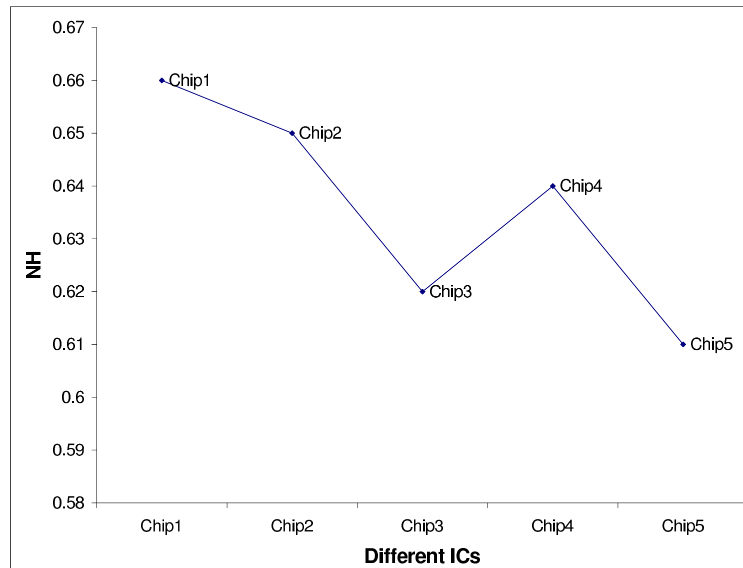


Figure 4.39: Minimum detectable NH obtained for the low level monitor in different chips.

- The noise pulse generator is selected to generate overshoots.
- No external stimuli is applied in order to generate the noise-free SUV at 640MHz.
- Applying frequency 1 and 2, the monitor outputs $OUTX$ and $OUTXN$ are observed
- External stimuli is applied in order to produce overshoots at the low level of the SUV. These overshoots have enough magnitude to produce signal integrity violations.
- Applying sampling frequency 1 and 2, we inspect the monitor outputs $OUTX$ and $OUTXN$

The goal is to observe the low level monitor outputs when the SUV is free or with noise (overshoots) and to identify when a signal integrity violation has occurred.

The following measurements are presented:

1. Noise-free at coherence frequency 1, fclk=8.88MHz

2. Noise-free at coherence frequency 2, fclk=13.6MHz
3. With noise pulse at coherence frequency 1, fclk=8.88MHz
4. With noise pulse at coherence frequency 2, fclk=13.6MHz

The first two show the dynamic performance of the low level monitor for two different coherent relations chosen for the sampling frequency. The next two show the behavior under a noise pulse for the two previously chosen coherent relations. The used noise pulse estimated from simulations has a height (NH) of 1.3 Volts and a width (NW) of 427ps. Fig. 4.40 shows the shape of the noise pulse obtained by electrical simulation.

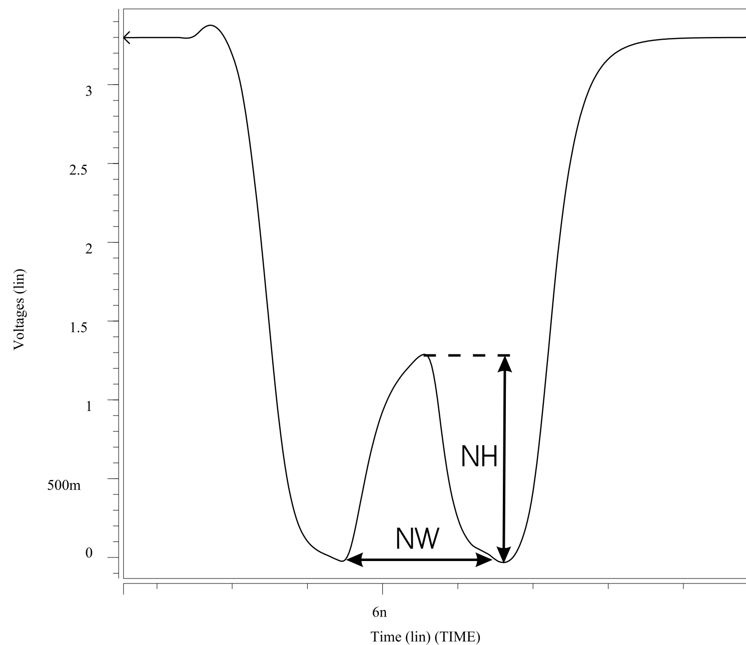


Figure 4.40: Shape of the noise pulse injected in the SUV in its low logic level.

Let's explain the expected results before to show the measurements. The response of the low level monitor (See Fig. 4.20) depends on of the sampling frequency (See the section of coherent sampling on Chap. 3). When the SUV has not integrity violation its outputs behavior is as follows: The node $OUTX$ remains in a high logic state while the SUV is sampled in the high

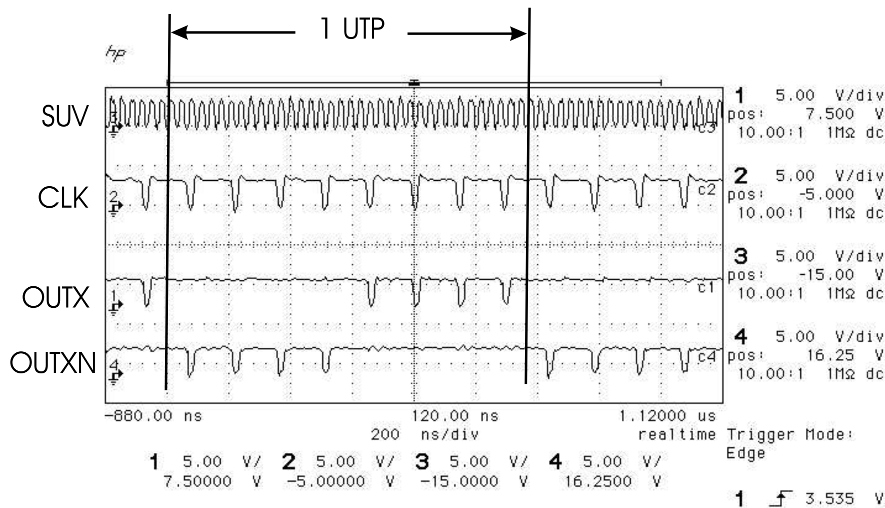


Figure 4.41: Output of the low level monitor when the SUV are free of noise and 8 samples are taken into the UTP, $f_{SUV} = 640MHz$, $f_{CLK} = 8.88MHz$.

logic state. When the SUV is sampled in the low logic state the node $OUTX$ presents pulses if the SUV does not have a signal integrity violation (overshoots). Fig. 4.41 shows the measurement 1 made to the low level monitor when the SUV is free of noise and 8 samples are taken into the UTP. The upper signal is the SUV frequency divided by 16, internally the SUV has a frequency of 640MHz. The next signal is the sampling signal (CLK), here it is important to note that due to coherent sampling inside of the UTP just 8 samples of the SUV have been taken, the sampling frequency is 8.8MHz. The next signal is the signal at node $OUTX$. From left to right, in the first 4 samples $OUTX$ remains to a logic 1 indicating that the SUV is sampled in the high logic state and the last 4 samples the node $OUTX$ presents pulses indicating that the SUV is sampled in the low logic state. Because the SUV is free of noise the last 4 samples produces four pulses in the node $OUTX$. The last signal is the signal in the node $OUTXN$ which has a complementary behavior of the node $OUTX$.

In the measurement 2, the number of samples taken to the SUV are increased. For taken 12 samples to the SUV, a sampling frequency of 13.6 MHz is used. The case for the noise-free SUV is shown in Fig. 4.42. From the upper to lower signal are shown SUV, CLK, OUTX, and OUTXN respec-

Figure 4.42: Output of the low level monitor when the SUV are free of noise and 12 samples are taken to the SUV in one UTP, $f_{SUV} = 640MHz$, $f_{CLK} = 13.6MHz$.

tively. At the beginning of the UTP from left to right, one sample is taken in the low logic level of SUV, hence the node $OUTX$ presents a pulse. In the next seven samples the SUV are sampled in the high logic level, hence the node $OUTX$ remains in a logic 1, in the last four samples the SUV are again sampled in the low logic level. Because the SUV is noise-free, all samples in the low logic level of SUV produce pulses in the node $OUTX$. It is important to note that seven samples are taken in the high and only five samples in the low logic levels of the SUV.

When a noise pulse is injected to the SUV, it will be detected by missing pulse when the SUV is sampled in the low logic state. The overshoot in the SUV is generated by the noise pulse generator. The magnitude of the overshoot is controlled by the external DC signal Vp that in this case is the 2V. The measurement results shown in Fig. 4.43 depict the results of measurement 3 for the SUV with integrity violation. The upper signal is the SUV divided in frequency by 16, the next signal is the sampling frequency (CLK), with this sampling frequency 8 samples are taken to the SUV, the next signal (OUTX) shows the behavior of the node $OUTX$. From left to right into the UTP, in the first 4 samples of the SUV, the node $OUTX$ re-

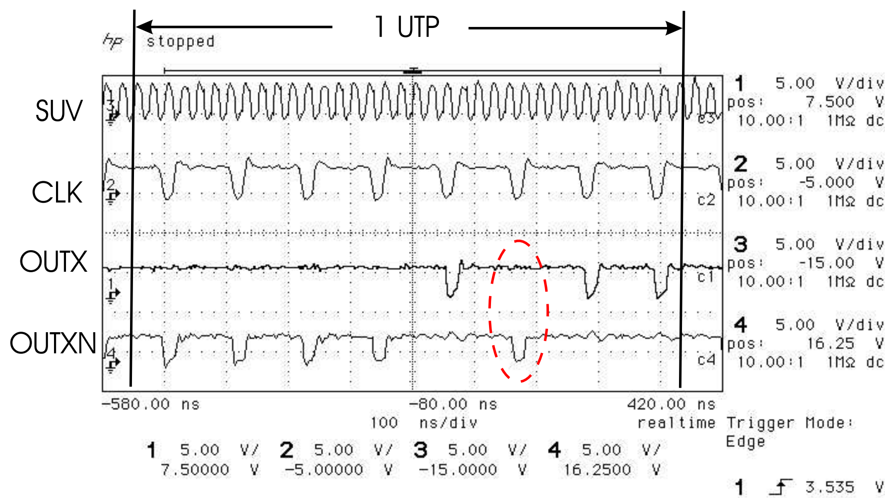


Figure 4.43: Output of the low level monitor when the SUV has a noise pulse and 8 samples are taken into the UTP, $f_{SUV} = 640MHz$, $f_{CLK} = 8.88MHz$, NH=1.3V, NW=427ps.

mains to logic 1 because the SUV is sampled in the high logic level. When the SUV with noise is sampled in the low logic state occurs a signal integrity violation which is detected by the monitor. It can be seen in the sixth sample of the SUV that the node $OUTX$ remains to a 1 logic and the node $OUTXN$ (lower signal) presents a pulse At the two next sampling periods the node $OUTX$ presents pulses and the node $OUTXN$ remains to a logic 1.

The measurement 4 results (See Fig. 4.44) are presented for the same noise pulse conditions. In this case, the number of samples taken to the SUV is 12. From the upper to lower signal are shown the SUV, CLK, $OUTX$, and $OUTXN$ respectively. The first 5 samples in the UTP (from left to right) are taken in the low level of the faulty SUV. In the first sample the low level monitor does not detect the overshoot, but in the second, third and fourth samples the overshoot is detected. In these samples the node $OUTX$ remains in a logic 1 and the node $OUTXN$ presents pulses. This output behavior indicates that a signal integrity has been detected by the low level monitor. In the fifth sample the SUV is still sampled in the low logic level but in this part the overshoot is not detected. In the last seven samples the SUV with noise is sampled in the high logic level, hence $OUTX$ remains in a logic 1

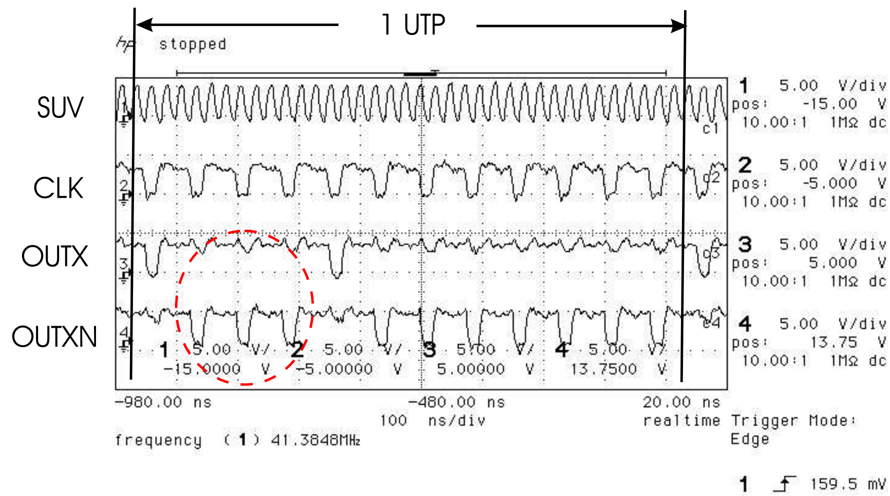


Figure 4.44: Output of the low level monitor when the SUV has a noise pulse and 12 samples are taken into the UTP, $f_{SUV} = 640MHz$, $f_{CLK} = 13.6MHz$, NH=1.3V, NW= 427ps.

and $OUTXN$ presents pulses.

4.3.3 Measurement to the module of the high frequency of the SUV, $f_{SUV} = 917MHz$

The measurements presented in this subsection is to observe the dynamic behavior of the low level monitor when it verify signals at 917MHz. The following steps are made in order to accomplish this:

- The internal VCO for the module of the high frequency of the SUV frequency is activated.
- Two coherent sampling frequency (frequency 1 and 2) are found in order to obtain 8 and 12 samples in one unit test period (UTP). Four and six samples are taken in the low and high logic level of the SUV for frequency 1 and 2 respectively.
- No external stimuli is applied in order to generate the noise-free SUV at 917MHz.

- Applying frequency 1 and 2, the monitor outputs $OUTX$ and $OUTXN$ are observed
- External stimuli is applied in order to produce overshoots at the low level of the SUV. These overshoots produce signal integrity violations.
- Applying sampling frequency 1 and 2, we inspect the monitor outputs $OUTX$ and $OUTXN$

The monitor outputs are inspected in order to identify signal integrity violations. In the module of the high frequency of the SUV, the highest frequency achieved is 917MHz. At this frequency two coherent relation have been considered in order to validate the low level monitor performance. Four measurement results are presented:

1. Noise-free at coherence frequency 1, fclk=6.8MHz
2. Noise-free at coherence frequency 2, fclk=13.6MHz
3. With noise pulse at coherence frequency 1, fclk=6.8MHz
4. With noise pulse at coherence frequency 2, fclk=13.6MHz

The first two measurements made for the noise-free SUV show the dynamic performance of the low level monitor for two different coherent relations chosen for the sampling frequency. The next two show the behavior under a noise pulse for the two previously chosen coherent relations. The used noise pulse estimated from simulations has a height (NH) of 1 Volts and a width (NW) of 198ps.

Fig. 4.45 shows the measurement 1 results for the case of the noise-free SUV where 8 samples are taken into the UTP. In the first 4 samples from left to right the SUV is sampled in its low logic level and because the SUV is noise-free, $OUTX$ presents pulses on each CLK period and $OUTXN$ remains to a logic 1. In the last 4 samples the SUV is sampled in its high logic level, in these samples $OUTX$ is a logic 1 and $OUTX$ presents pulses.

Fig. 4.46 shows the measurement 2 results for the case of the noise-free SUV when 12 samples are taken into the UTP. The sampling frequency is 13.6MHz. From left to right, the first four samples are taken in the low

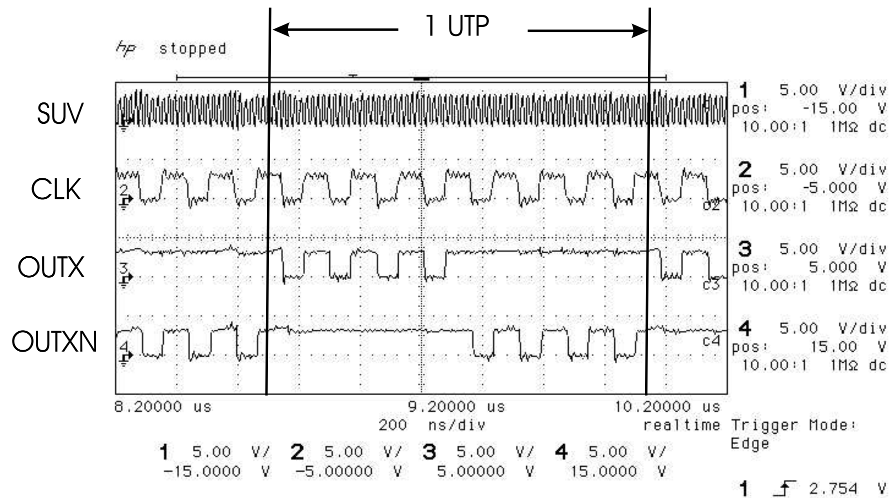


Figure 4.45: Measurement of the low level monitor response in the case of the noise-free SUV. 8 samples are taken into the UTP at rate of $f_{SUV} = 917MHz$, $f_{CLK} = 6.8MHz$.

logic level of the SUV, hence the node $OUTX$ presents pulses and the node $OUTXN$ remains to 1 logic. This behavior indicates that there is not integrity violation of the SUV. In the last eighth samples the noise-free SUV is sampled at its high logic level, hence $OUTX$ remains to a 1 logic and the node $OUTXN$ presents pulses.

For the case of the SUV with noise an overshoot has been generated by the noise pulse generator in the low logic level of the SUV. Two coherent relations have been also used to validate the performance of the low level monitor for this case. Fig. 4.47 shows the measurement 3 results for the case of the verification of the SUV when 8 samples are taken into the UTP. From left to right, the first 4 samples are taken in the high level of the SUV with noise, hence $OUTX$ remains to a logic 1 and $OUTXN$ present pulses. In the last 4 samples the SUV is sampled at its low logic level. In the sixth and seventh samples into the UTP the low level monitor detects an integrity violation. The node $OUTX$ is a logic 1 and the node $OUTXN$ presents a pulse in those samples.

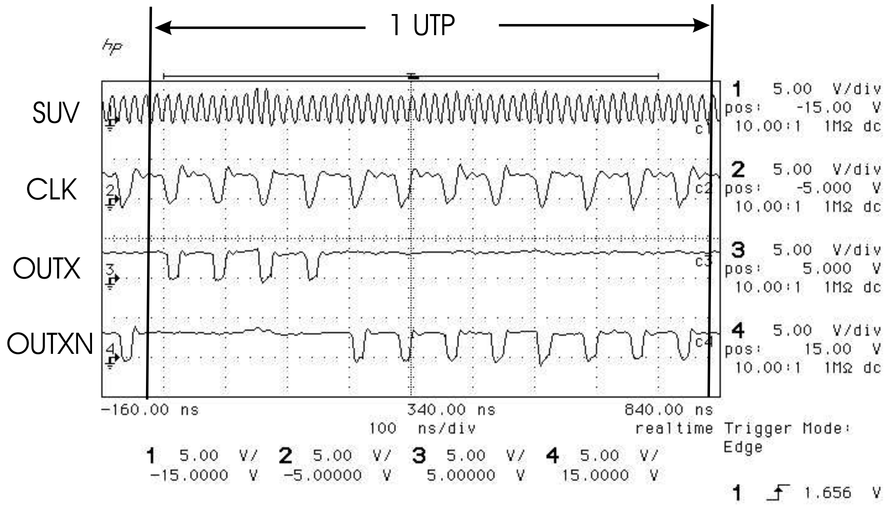


Figure 4.46: Measurement of the low level monitor response in the case of noise-free SUV. 12 samples are taken into the UTP, $f_{SUV} = 917MHz$, $f_{CLK} = 13.6MHz$.

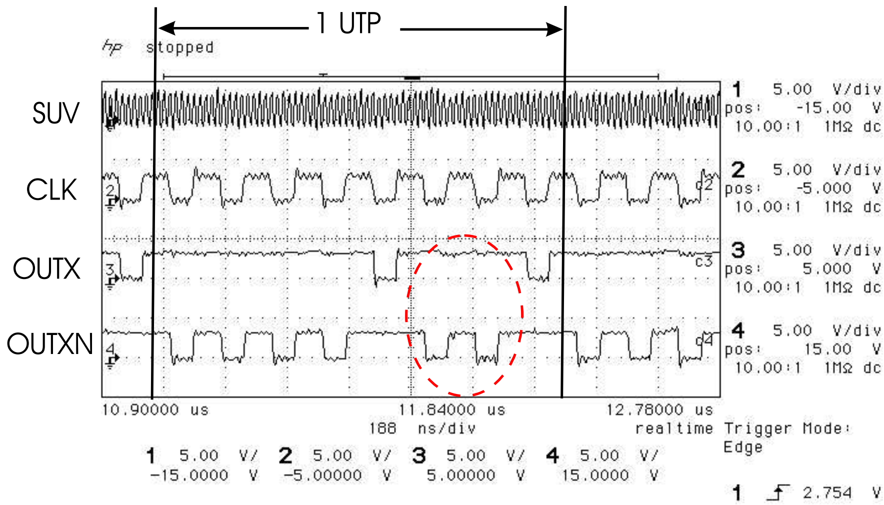


Figure 4.47: Measurement of the low level monitor response in the case of the SUV with signal integrity degradation. 8 samples are taken into the UTP, $f_{SUV} = 917MHz$, $f_{CLK} = 6.8MHz$, NH=1V, NW=198ps.

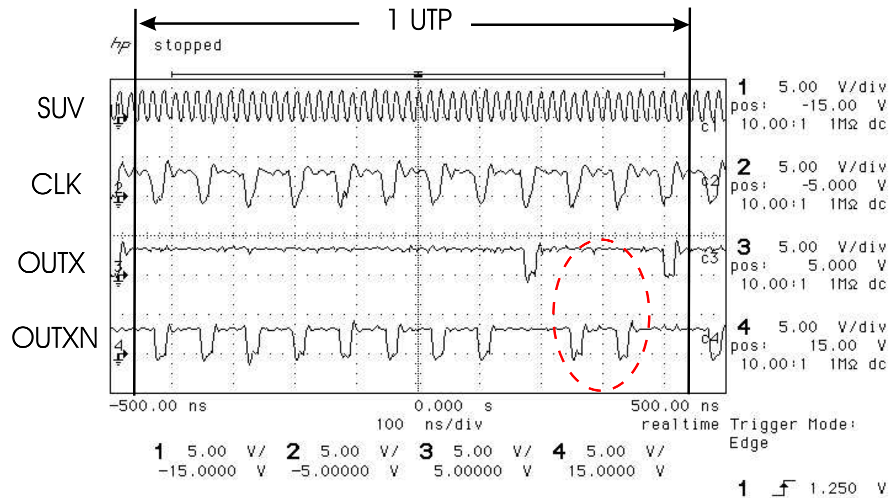


Figure 4.48: Measurement of the low level monitor response in the case of SUV with signal integrity degradation. 12 samples are taken into the UTP, $f_{SUV} = 917MHz$, $f_{CLK} = 13.6MHz$, NH=1V, NW=198ps.

Fig. 4.48 shows the measurement 4 results for the case of SUV with noise when 12 samples are taken into the UTP. The sampling frequency is 13.6MHz. From left to right, in the first eighth samples the SUV is sampled in the high logic level, hence $OUTX$ remains to a logic 1 and $OUTXN$ presents pulses. In the next four samples the SUV is sampled in the low logic level. In the tenth and eleventh samples the overshoot is detected. $OUTX$ is a logic 1 and $OUTXN$ presents two pulses in those samples. In the other samples in which the SUV is sampled in the low logic level (ninth and twelfth samples), $OUTX$ presents pulses. This section has presented measurements for the DC and the dynamic behavior of the low level monitor. With DC behavior, the detectable voltage level for the fabricated low level monitor is found.
Two different sampling frequencies are applied. The low level monitor verify signals at 640MHz and 917MHz. For the sampling frequency 1 and 2, 8 samples were taken for SUV at 640MHz and 917MHz.
If the SUV is noise-free, the node $OUTX$ presents 4 and 6 pulses when the SUV is sampled in the low logic level and $OUTXN$ presents no pulses for frequency 1 and 2 respectively. When the SUV is sampled in the high logic level, node $OUTX$ presents no pulses and node $OUTXN$ presents 4 and 6 pulses for frequency 1 and 2 respectively. If the SUV presents overshoots

which generates integrity violations and the sampling frequencies 1 and 2 are applied, node $OUTX$ presents less than 4 or 6 pulses when the SUV is sampled in the low logic level for sampling frequency 1 and 2 respectively. We conclude that a missing pulse or pulses when the SUV is sampled the low logic level indicates a signal integrity violation. The number of missing pulse is increased when the magnitude and duration of the overshoot is increased.

4.4 Estimation of the noise pulse width injected to the SUV

The noise pulse applied to the SUV is generated and injected internally. Indirectly the duration of this noise pulse (NW) can be estimated by using the resolution of the coherent sampling and the number of the detections of integrity violations into the UTP. When the effective sampling resolution (T_r in time) has the characteristics shown in Fig. 4.49, it means that the noise pulse duration is almost equal or slightly longer than the effective sampling resolution. If one detection of the noise pulse is made by the monitor under this condition, it is possible to assure that the noise pulse width is given by the following relation:

$$T_r \leq NW < 2T_r$$

Because only one detection is found, the NW must be smaller than $2T_r$. If NW is longer than $2T_r$ two detection must be found. The sample at time t_0 in Fig. 4.49 is a sample taken outside of the the noise pulse and it is not detected by the high level monitor. The sample at time t_1 is a sample taken into the noise pulse and it is detected by the high level monitor. The sample at time t_2 is again taken outside of the noise pulse and it is not detected by the high level monitor. If more detections are found by the monitor it means that the effective sampling resolution is smaller than the noise pulse width. For two samples taken into the noise pulse, two detection are made by the high level monitor, it is possible to estimate the approximate duration of the noise pulse width with the following relation:

$$2T_r \leq NW < 3T_r$$

Fig. 4.50 depicts this case. The samples taken at the times t_1, and t_2 are into the noise pulse, these samples are detected by the high level monitor,

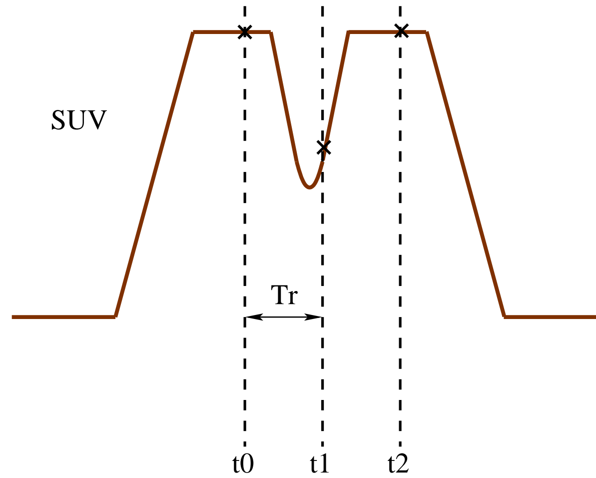


Figure 4.49: Example of one detection made by the high level monitor. The duration of the noise pulse is approximate the effective sampling resolution

the samples taken at times t_0 and t_3 are outside of the noise pulse and these samples are not detected by the monitor. It is possible to build a general relationship for the estimated duration of the noise pulse width as follows:

$$kT_r \leq NW < (k+1)T_r \tag{4.1}$$

Where k is the number of samples taken into the noise pulse and which generates detections in the monitor.

The simulated values of the noise pulse height and width (NH and NW respectively) for different Vn DC stimuli voltages and the SUV frequency at 640MHz are shown in table 4.4.

DC stimuli	NH	NW
0v	0	0
0.6v	0	0
1	0.92V	246ps
1.5v	1.11V	401ps
2v	2V	442ps

Table 4.4: Values of the noise pulse height and width injected to the SUV obtained by simulation.

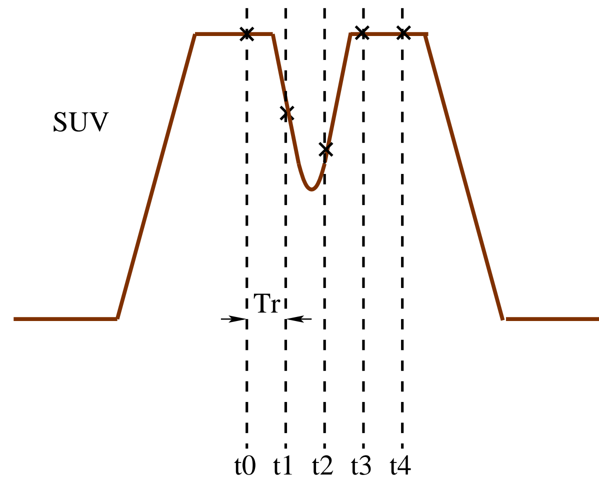


Figure 4.50: Example of two detections made by the high level monitor. The duration of the noise pulse is approximate two times the effective sampling resolution.

For the case of the SUV at 640MHz, 16 samples have been taken into the UTP, the effective frequency resolution (T_r) is the 97.6psec, the actual sampling frequency is 17.74MHz, and different DC stimuli voltages are applied to the noise pulse generation (Vn). The experimental estimated noise pulse width injected to the SUV applied to the high level monitor are shown in table 4.5. The values of NW is estimated by multiplying the number of de-

DC stimuli	# detections	NW
0v	0	0
0.6v	0	0
1	2	195.2ps
1.5v	4	390.4ps
2v	5	488ps

Table 4.5: Experimental estimation of the noise pulse width injected to the SUV for the case of 16 samples.

tections of the signal integrity violations by the effective sampling resolution. These values fall into the range given by Eq. 4.1. If the coherent sampling resolution is increased we can obtain a better estimation of the noise pulse width than the case of 16 samples into the UTP. For the case of 32 samples

into the UTP. The actual sampling frequency is 35.5MHz, and the effective sampling resolution is 48.28ps. For different DC stimuli voltages applied to the noise pulse generation, the table 4.6 shows the NWs obtained:

DC stimuli	# detections	NW
0v	0	0
0.6v	0	0
1v	4	193.12ps
1.5v	9	434ps
2v	10	483ps

Table 4.6: Experimental estimation of the noise pulse width injected to the SUV for the case of 32 samples.

4.5 Conclusions

Experimental measurements of the behavior of the proposed monitors have been presented. The monitor responses for the cases of the fault-free and faulty SUV have been analyzed for different frequencies. The high and low level monitor performances have been presented by measurements in DC. These measurements allows to estimate the magnitude of the noise pulse detected by the monitors. The DC measurements are close to the value predicted by simulation for the case of the longest noise pulse duration. The dynamic performance of the monitor has been also presented. It is shown that the monitors detect the integrity violation at different rates of SUV and for different coherent relation of the sampling signal.

Measurements of the monitors responses verifying the SUV at frequencies of 320MHz, 640MHz and 917MHz and two sampling frequencies have been presented. It has been shown that the monitors allow to detect undershoots and overshoots in the signal under verification at different rates. Using the coherent sampling we can increase or decrease the resolution of the information taken to the SUV. The selected resolution is according to the requirements of the signals. For example, if the noise pulse width to detect is 100psec, the resolution of the coherent frequency must be smaller than 100psec. Into the chip fabricated the maximum SUV frequency generated is 1.8GHz, but due to the noise pulse generator circuitry the maximum SUV frequency was

limited to 917MHz. This issue is due to the constraint of using very fast circuits to inject the noise to the SUV.

Chapter 5

Conclusions

The scope of this thesis is to analyze and propose a methodology to verify the signal integrity of on-chip interconnects. It is proposed to use the dominant poles in order to have a first order model to determine if the signal has an acceptable or unacceptable integrity quality. The case of a data bus including shielding lines is analyzed to observe the interconnect coupling impact on signal integrity when a shielding line presents an open defect. A novel methodology to verify the signal integrity of on-chip interconnect lines has been proposed. The proposed technology allows to have high resolution for assuring high quality of the signals. Monitors to sense the signals under verification using an undersampling scheme have been proposed.

It has been demonstrated that if the shielding line presents a open defect its shielding effect is degraded. Hence, the protected signal propagating in an adjacent metal line can present ringing affecting the signal quality. It is shown that the loci of the extracted poles of the signal ringing can be used as a first order model to know if the signal has an acceptable or unacceptable integrity quality. By electrical simulations, we extract the dominant pole of the ringing frequency and observe their loci for different interconnect lengths and resistive opens. For a given interconnect length and varying the value of the resistive open of the shielding line, we obtain the pole loci for each resistive open value. These pole localizations define two regions. In one of them, the signal integrity still has an acceptable integrity quality for certain resistive open values, and in the other one the signal has not an acceptable integrity quality. The experiment was made for different size characteristics of the transmitter and receiver driver. It is shown that the driver size also

impact the signal integrity quality. In high performance systems, critical signals need to be verified. Unacceptable ringings can occurs in the logic states of the signal under verification.

A methodology to verify unacceptable ringings in the high (undershoots) and low (overshoots) logic levels of high speed digital signals has been presented. Two monitors are used to sense signal integrity violations, the high level monitor senses the unacceptable undershoots and the low level monitor senses the unacceptable overshoots. The detectability of the monitor depends on the undershoot and overshoot characteristics. The monitor performance has been evaluated with the voltage magnitude (NH) and the time duration (NW) of the undershoot and overshoot pulse (noise pulse). The monitors have been designed to obtain the detection of the smallest NW possible. For the smallest NW, the highest NH is required to be detected for the monitors. The detectable value of the NH decreases when the NW increases. For long durations of the NW the magnitude of the NH remains almost constant, it can be considered as the minimum NH detectable for the monitors.

The monitors use the coherent sampling scheme to verify the signal under verification. The half period of the sampling signal (CLK) is used to precharge (discharge) the high (low) level monitor to VDD (GND). The other part of the CLK period is used to verify the signal. The sampling scheme allowed to obtain information of the entire signal under verification with N samples at relatively smaller frequency rates. It was achieved by establishing the coherent relation between the frequencies of the signal under verification and CLK. When the coherent relation is established, the entire information of the signal under verification is taken in N samples of M periods of the signal under verification. N and M are integer relative prime numbers and in all coherent relations M is higher than N. This allows to have a relatively small sampling frequency.

The proposed monitors can be designed to verify more than two signals. The number of those signals to verify is limited only for the features of the undershoots and overshoots to verify. The monitor designed to verify multi-signals may detect noise pulses with more duration than the monitor designed to verify only one signal. The proposed methodology assure not losing information of the samples taken of the signal under verification.The change from

one to other signal under verification is made without losing information. To accomplish this, two enable signal generators are required, one for each monitor. These enable signal generators activate the monitor to verify only one signal in each UTP. Before the end of each UTP the monitors must be ready to verify the next signal.

The UTP is divided in two parts, one of them is to verify the high logic level of the signal under verification. In this part only the information generated by the high level monitor is analyzed. The other part of the UTP is to verify the low logic level of the signal under verification hence, only the information generated by the low level monitor is analyzed. Additional circuitry has been implemented to detect the start and the end of each part of the UTP. At the end of the part of the UTP used to verify the high logic level, the circuitry generate a flag signal. This flag signal is sent to the enable signal generator. With this, the high level monitor is prepared to verify the next signal by activating the corresponding enable signal.The same occurs for the low level monitor. When this circuitry detect the end of the UTP part, it is used to verify the low logic level of the signal under verification.In each UTP part, the monitor output is stored in one flip-flop which output is sent-out to an external pin.

The methodology accuracy is affected by the CLK and SUV jitter. Limits of jitter values are established to assure a good performance of the methodology. The signal under verification (SUV) can suffer of jitter but, in combination with the clock jitter, the total amount of jitter accumulated must be equal or smaller than the amount established by equation (5.1).

$$\Delta T_{jitter} = (K - 1)r \tag{5.1}$$

A prototype circuit to validate the proposed methodology has been designed and fabricated. Special circuits to systematically injects noise pulse were designed. Two modules have been generated with these circuits. One module is able to generate SUV frequencies from 100MHz to 640MHz. The other module was designed to verify as signal at a frequency of 917MHz. The measurements of the fabricated high and low level monitors validate the feasibility of these monitors to verify signal integrity violation in high speed signals. The experimental measurements shows a good agreements with the

simulations results. Measurements for both monitors at different coherent sampling rates have been presented. With each sampling rate, the cases for the noise-free and with noise signal under verification are presented. The proposed methodology has been validated for different frequencies.

Appendix A

Two-Bit counter performance

The reset action would be taken when the two-bit counter gives the count of 11 and in the next CLK period. The proposed two-bit counter is depicted in the Fig. A.1, this counter consist of two toggle flip-flops and the additional circuitry needed to do the reset action. The goal of this counter is to have a unique initial state (0 0) at the beginning of the methodology, then the next counts (0 1), (1 0), and the last (1 1) will take place in each logic change of ER signal. At this point, count (1 1), the counter is able to change its binary count from (1 1) to (0 1) in the next CLK period where the signal C_1 has the same logic value that the signal ER and hence the signal Xor-out becomes a logic 0. In the count (1 1) the signal f_2 is high and when Xor-out is low a reset signal is activated. This reset signal is the result of the NAND function of f_2 and Xor-out (see Fig. A.1). The reset signal toggle the HSB flip-flop to a logic 0 but the bit stored in the LSB flip-flop holds on 1 logic. These actions set the count of the two-bit counter in (0 1) before that signal ER changes its logic value.

A timing diagram to clarify the behavior of the two-bit counter is shown in Fig. A.2. Let's assume that the counter has the binary number (1 0) and that in the next CLK rise edge goes to (1 1) as Fig. A.2 shows. At time t_{c1} CLK is high and the logic change of ER is detected by the Xor gate which commute from 0 to 1. The Xor gate switching action makes the two-bit counter counts to (1 1) (Signals LSB and HSB are high in the timing diagram) and due to this count the signal f_2 becomes high.

At t_{c2}, the next CLK rise edge, the signal Xor-out is going to a logic 0 because the Xor inputs (C_1 and ER) have the same logic value, at this moment with Xor-out low and f_2 high, the signal C_f becomes low (at time

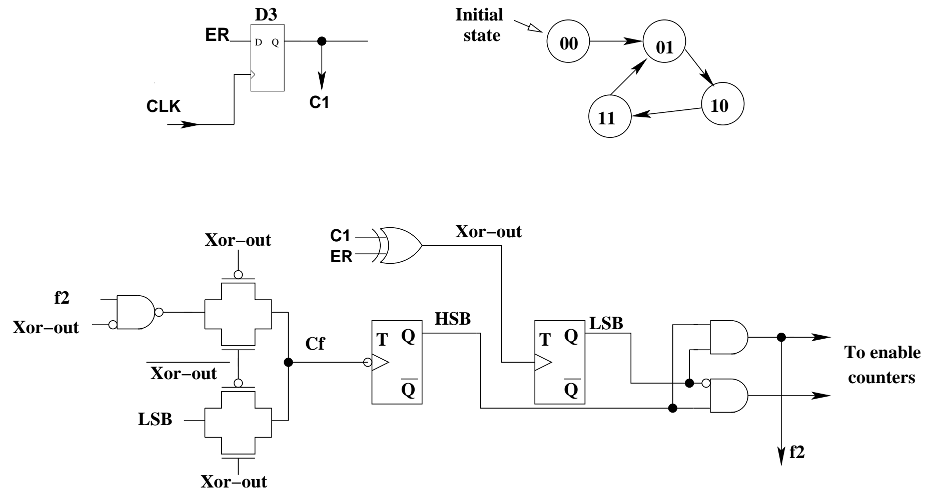


Figure A.1: Proposed two-Bit counter is implemented by additional circuitry in order to achieve the needed count.

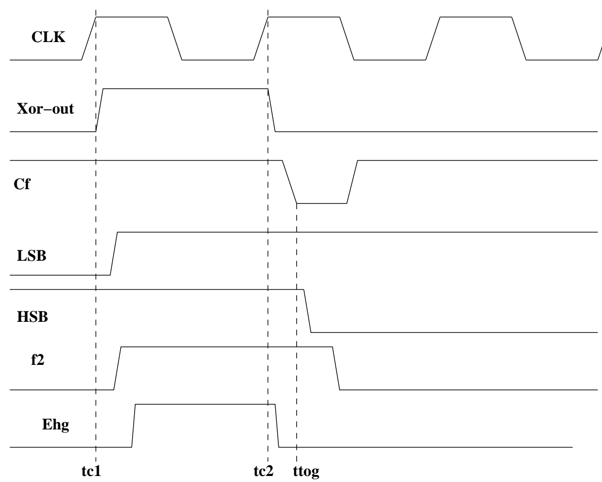


Figure A.2: Timing curves explain the two-bit counter performance.

t_{tog}) and toggle the HSB flip-flop from logic 1 to logic 0 when the signal HSB change to 0 it is detected by the AND gate hence its output f_2 change to 0 commuting the signal C_f to a high logic state and leaving the binary count in (0 1) ready for the next logic change of ER signal in which the two-bit counter counts the binary number (1 0). This binary number indicates the end of the high part of ER and prepares the enable signal generator to turn-off the signal E_{2h} and turn-on the signal E_{3h} for the next test period. In the next logic change of E_r the two-bit counter computes the binary number of (1 1) which will activate the signal E_{3l} and again the counter will be reset to (0 1) and will continue counting until the last signal has been verified. Fig. A.3 shows the simulation performance of the two-bit counter. The counter is set with each pulse at the XOR output. When the counter counts the binary number **11** means that one UTP has finished. At this point the counter is reset to the binary number **01** that indicates the first change of the new UTP.

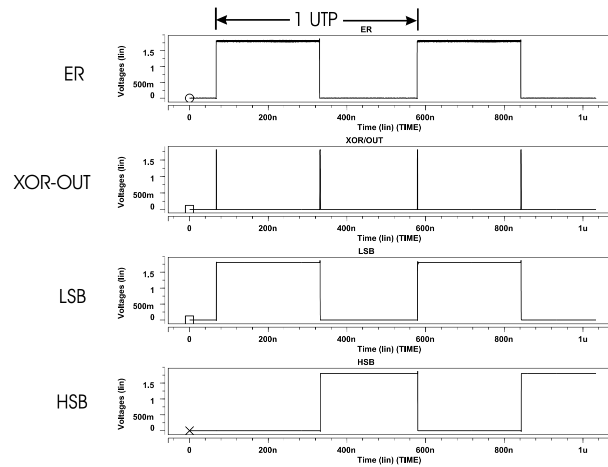


Figure A.3: Simulation performance of the two-bit counter. The initial state of the two-bit counter is **00**. The counter counts with each pulse at the XOR output.

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Resumen

El diseño de circuitos integrados ha evolucionado en gran medida gracias a los avances de la industria de semiconductores. Estos avances han permitido que la capacidad de integración de dispositivos dentro de un solo circuito integrado (CI) haya aumentado en grandes proporciones. Es posible implementar una gran cantidad de bloques dentro de un CI para que realicen diversas funciones. Tener un CI que realice varias funciones abarata los costos lo cual es un aspecto atractivo para los consumidores. La integración de sistemas dentro de un chip y el aumento de la frequencia de reloj permiten tener circuitos integrados de altas prestaciones. Realizar varias funciones a altas velocidades es una caraterística importante y necesaria en el desarrollo de productos electrónicos con tecnologías actuales.

Circuitos integrados con gran cantidad de bloques funcioneles y además trabajando a frequencias en el orden de gigahertz generan una serie de problemas que deben de ser tomados en cuenta por el diseñador de CIs. Los bloques digitales dentro de un CI son una gran fuente generadora de ruido. Este ruido generado por las rápidas transiciones de las puertas lógicas, pueden causar un mal funcionamiento a bloques funcionales analógicos sensibles a tales ruido. Otro problema, que se deriva de la gran capacidad de integración, son las interconexiones dentro del CI. Tecnologías actuales han reducido el ancho de las interconexiones, permitiendo tener líneas de interconexión más cerca una de otras. Esto resulta en una gran densidad de líneas de interconexión a lo largo y ancho del CI. También se puede agregar que es posible tener 7 niveles de metal en CI lo cual aumenta aún más el número de líneas.

Las líneas de interconexión transportan señales de un bloque funcional a

otro a distancias que pueden ser de unos cientos de micras a varios milímetros. La frequencia de las señales transportadas en estas líneas de metal está en el rango de los gigahertz. A estas frecuencias, los efectos electromagnéticos pueden producir degradación en la integridad de la señal. Violaciones a los niveles de integridad de señal establecidos para un buen funcionamiento son producidos por varias fuentes de ruido.

El ruido de sustrato es un problema importante porque afecta a circuitería sensible a ruido tales como bloques analógicos. Cuando un circuito digital conmuta, una corriente es inyectada hacia el susbtrato por medio del acoplamiento de las líneas de interconexión y de los dispositivos. La gran cantidad de dispositivos conectados a la línea de alimentación incrementa el consumo de corriente en diferentes puntos de la línea de alimentación. Esto ocaciona una caida del nivel de voltaje de la alimentación provocando una degradación en el funcionamiento de los circuitos, un incremento en el retardo de las señales y reducción en el margen de ruido.

La interconexiones juegan un importante rol en la integridad de la señal. Líneas de interconexión en CIs actuales viajan a lo largo del CI con una separación muy pequeña lo cual produce un acoplamiento capacitivo importante. Además en sistemas de altas prestaciones el acoplamiento inductivo entre interconexiones es significativo y la inductancia total de la línea debe de ser tomada en cuenta. Un modelo apropiado debe de realizarce de los parámetros de las líneas de interconexión para evaluar el funcionamiento de circuitos que trabajan a altas velocidades. Una línea de transmisión puede ser modelada con un simple circuito concentrado RLC. Un forma más exacta de modelar una línea de transmisión es por medio de un modelo distribuido. En este tipo de modelo las características de la línea es dividida en varias etapas.

En todos los casos de modelado de las líneas de transmisión exite solamente una trayectoria de polos dominantes. Los polos dominantes tienen sus raices cercanas a el eje imaginario del plano complejo y con frequencias de oscilación menores que las demás trayectorias. Un par de polos que dan información importante de la línea de transmisión, corresponden a un sistema de Segundo grado. Los valores de undershoots y overshoots pueden ser estimados por medio de la aproximación de los polos dominantes.

Para reducir el acoplamiento capacitivo e inductivo entre líneas de interconexión se utilizan líneas de protección. Cuando estas líneas de protección son insertadas entre dos líneas de señal, el acoplamiento capacitivo es reducido al máximo. La inductancia de las líneas es también reducida al generar un camino de retorno de corriente más cercano a la línea de señal. Defectos en las líneas de protección pueden generar degradación en la integridad de la señal en una línea que viaje adyacente a ella. El mapeo de los polos dominantes de las señales que viajan en las líneas de interconexión indican si esta ocurriendo una violación de la integridad de la señal. Regiones de aceptable y no aceptable integridad de señal pueden ser establecidas con este mapeo de polos dominantes.

En señales digitales fluctuaciones de voltage (ringings) en los estados pueden generar falsas transiciones en los receptores que son alilmentados con estas señales. Ringings en el estado lógico alto de la señal son llamados undershoots y en el estado bajo overshoots. En el presente trabajo se propone una nueva metodología de verificación de integridad de señal. Dos monitores son propuestos; uno para verificar el estado alto de la señal y otro para el estado bajo.

Las señales son verificadas bajo es esquema de muestreo coherente. Este esquema de muestreo permite tomar información de la señal bajo verificacion (SBV) a relativamente baja frequencia y con una alta resolución entre muestras. Alta resolución significa tener muestras de la señal muy cercanas. Es posible implementar estos dos monitores para la verificación de más de dos SBV. Para realizar la verificación de una señal es necesario establecer una ventana de prueba. En esta ventana de prueba la SBV se va a repetir M veces y serán tomadas N muestras. Los valores de M y N son tomados de acuerdo a una relación de coherencia necesaria para tomar la mayor información posible de la SBV. El valor de N es menor que M. La información obtenida en una ventana de prueba corresponderá a la de un periodo de la SBV.

Cada muestra tomada de la SBV en la ventana de prueba es verificada por ambos monitores, pero solo la información de uno es analizada. Es necesario identificar que estado lógico de la señal se está verificando para determinar

de que monitor se va a analizar la información obtenida. Una arquitectura de monitoreo es necesaria para realizar la identificación del estado lógico verificado. También es requerido conocer el final de la verificación de una señal para pasar a la verificación de otra y que esto no implique perdida de información.

Si se requiere verificar tres señales, tres ventanas de prueba son necesarias. Como la metodología utiliza muestreo para analizar a la SBV, la localización de las primeras muestras de la señal es desconocida. Hasta que occurre el primer cambio de estado de la señal muestreada se considera la información útil. El circuito orientado a generar el estado lógico en que se estan tomando las muestras es un flip-flop que tiene como entrada a la SBV y como reloj a la señal de muestreo. La salida de este flip-flop (ER) indica en que estado lógico se está muestreando la SBV. La señal ER es introducida a un circuito que va a indicar cuando existe un cambio lógico en esta señal y si la transición fue de alto a bajo o viceversa. Esta acción es útil para identificar cuando se ha comenzado y terminado de verificar un estado lógico. Una cuenta de estas transiciones ayuda a determinar cuando los dos estados lógicos han sido verificados de una SBV. La Fig. A.4 muestra el diagrama esquemático del generador de señales de habilitación.

Los dos monitores propuestos son utilizados para verificar una señal a la vez. Señales de habilitación son requeridas para determinar que señal va ser verificada. Cuando, por ejemplo, han ocurrido las primeras tres transiciones de la señal ER, significa que ya se ha terminado de verificar la primera SBV, en este momento es necesario habilitar al monitor para que verifique la siguiente SBV. Tres señales de habilitación son requeridas por el monitor de estado alto y bajo para verificar tres señales. Cuando se termina de verificar un estado lógico en una ventana de prueba, el monitor que verifica ese estado lógico debe de ser preparado para verificar la siguiente SBV para cuando inicie la siguiente ventana de prueba. Con esta acción se asegura que siempre al inicio de una nueva ventana de prueba los monitores estan listos para verificar la señal correspondiente.

Los monitores comparan a la señal bajo verificación (SBV) contra un voltaje de referencia. Para el monitor de estado alto el voltaje de referencia es V_{DD}

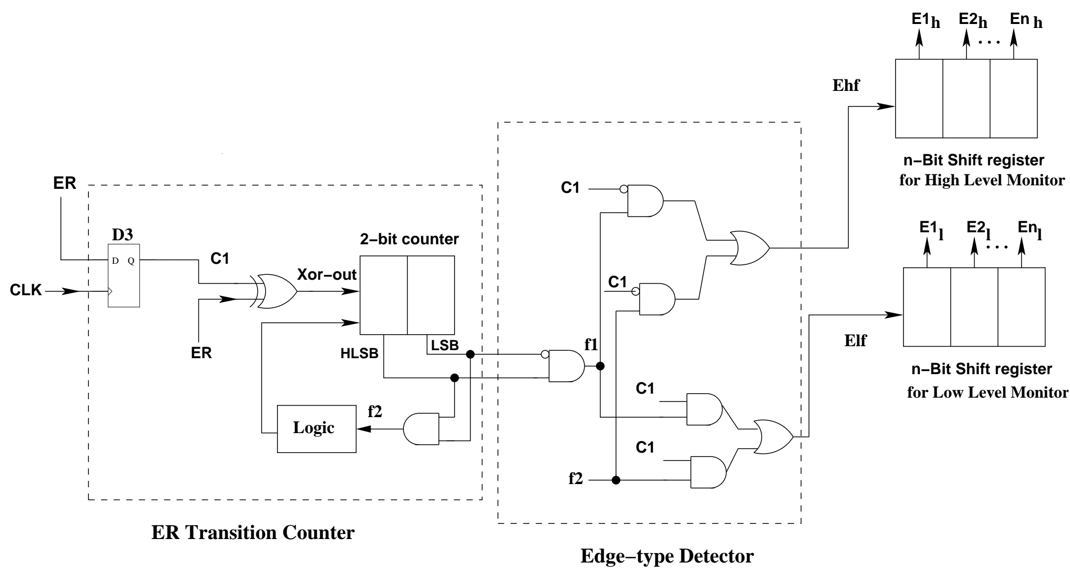

Figure A.4: Diagrama esquemático del generador de señales de habilitación.

y para el monitor de estado bajo el voltage de referencia es GND. En el caso de que estos voltajes de referencia sean tomados de la línea de alimentación y tierra del CI, el ruido que hay en ellas puede modificar el funcionamiento de los monitores. Una solución a este problema es la de aislar los voltajes de referencia de los demás circuitos del CI. Por medio de un interruptor se carga un capacitor a los niveles de V_{DD} o GND mientras los monitores no estan evaluando la integridad de la señal. En el momento de la evaluación el switch se abre quedando almacenado el voltaje de referencia en el capacitor y aislado de la red de alimentación del CI. Otra solución es la de dedicar una entrada de voltaje de referencia para cada monitor. Aunque esto implica incrementar el numero de pins del CI.

La exactidud de la metodología depende principalmente en el esquema de muestreo. El límite de la exactitud lo condiciona el nivel de jitter posible en la señal de muestreo. La resolución de muestreo (separación en tiempo entre muestras) debe de ser menor que el ancho del pulso de ruido que se pretende detectar con los monitores. Pero esta condición no basta para asegurar la detección de una violación de integridad de la señal. Si la especificaciones de integridad de señal establecen que un pulso de ruido (undershoot u overshoot) de duración NW debe de ser detectado como una violación de integridad de

señal, la resolución del muestreo debe de asegurar tener por lo menos K muestras dentro de ese pulso de ruido. El mínimo jitter permitido tiene que ser igual o menor a $\Delta T_{jitter} \leq (K-1)r$. Donde ΔT_{jitter} es la cantidad de jitter permitido, K es el numero de muestras tomadas dentro del pulso de ruido y r es la resolución de la señal de muestreo. Con esta expresión se asegura que con esa cantidad de jitter por lo menos una muestra será tomada dentro del pulso de ruido.

La metodología propuesta requiere de implementar diversos bloques dedicados al control de la metodología y el almacenamiento de la información. Esto implica costos desde el punto de vista de área, pins extras requeridos, el retardo que se añade al incluir la metodologia de verificación y el tiempo de verificación necesario para verificar todas las señales deseadas. Se ha realizado una estimación del costo en área de la metodología propuesta. Para implementar esta metodología de verificación en una tecnología de $0.18\mu m$ se requiere de 2300 μm^2. Esta área incluye dos monitores diseñados para verificar tres señales, la circuiteria de control utilizada y el almacenamiento requerido para la información obtenida de los monitores. Si se cuenta en el CI los medios adecuados para generar internamente la señal de muestreo, solamente es requerido un pin extra. Este pin extra es necesario para sacar la información obtenida por los monitores.

El retardo que se añade al incluir la metodologia es medido en porcentaje. este porcentaje esta en relación a la porción de retardo que es incluido por la metodología con respecto al retardo que sufre la señal al viajar por la línea de interconexión. La tabla A indica este porcentaje de retardo agregado por la metodología para diferentes longitudes de líneas de interconexión.

Los monitores propuestos fueron diseñados y fabricados en la tecnología de $0.35\mu m$. Fue necesario generar internamente la SBV con la finalidad de tener control sobre las características del pulso de ruido inyectado. Dos módulos fueron diseñados para comprobar la funcionalidad de los monitores propuestos a diferentes frequencias. Un módulo es capaz de generar señales para ser verificadas a frequencias desde 100MHz hasta 670MHz. La Fig. A.5 muestra el diagrama a bloques de este módulo. Se implementó un oscilador controlado por voltaje (VCO por sus siglas en ingles) interno para producir

Longitud(mm)	Retardo agregado
0.5	2%
1	7.1%
2	13.6%
3	13.5%
4	11.5%
5	8.8%
10	3.4%

señales en este rango de frequencias. Con el fín de observar externamente la frecuencia que se esta generando por el VCO, se diseño un divisor de frequencia. Una copia de la salida del VCO de este módulo es dividida entre 16 y enviada al exterior por medio de un pad. Esta división de frequencia es solo para aspectos de observación y de poder conocer la frecuencia que se esta generando en este módulo.

La señal generada por el VCO en el rango de frecuencias de 100MHz a 670MHz es la que será verificada por los monitores propuestos. A esta señal es necesario inyectarle pulsos de ruido en la parte lógica alta y baja para generar los undershoots y overshoots respectivamente. El generador del pulso de ruido es el encargado de inyectar los pulsos de ruido a la señal generada por el VCO. El generador de pulso de ruido fue diseñado para que trabajara correctamente en el rango de frequencias arriba mencionado. La señal de muestreo es introducida por medio de un pin del CI fabricado. Esto nos permite tener un control externo de la frequencia de muestreo y poder establecer la relación de coherencia.

El segundo módulo fabricado esta orientado a realizar la verificación de la señal a la más alta frecuencia posible. Se han utilizado los mismos bloques que en el caso del módulo 1 con la diferiencia de que para este módulo se han rediseñado los bloques para que trabajaran a la mayor frecuencia posible. La máxima frequencia lograda fue de 1.8GHz. A esta frecuencia no se logró que los bloques requeridos para inyectar el pulso de ruido funcionaran correctamente. Fue hasta una frecuencia menor que se logro generar las señales a verificar con pulsos de ruido controlables. La frecuencia en la que se logró esto fue a 917MHz.

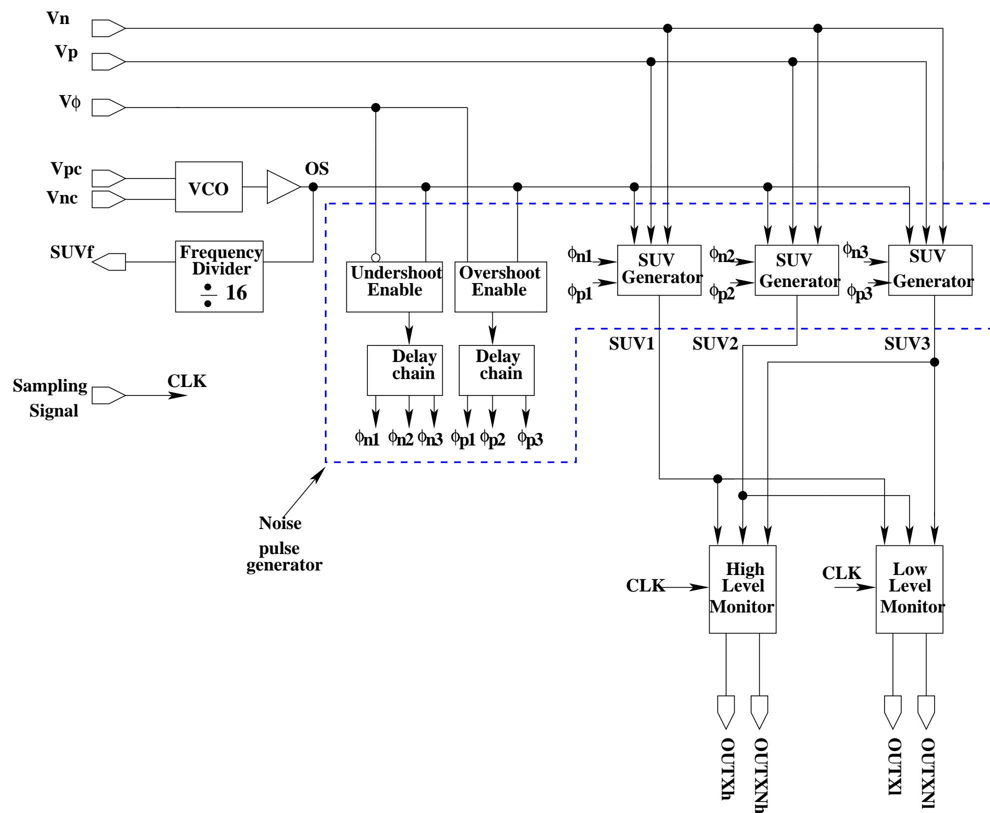

Figure A.5: Diagrama a bloques del módulo con frecuencia controlable de la señal bajo verificación.

Dos frecuencias de la señal a verificar (640MHz y 917MHz) se han escogido para realizar el conjunto de mediciones experimentales. Para ambas frecuencias de la señal se han verificado los casos con y sin violación de la integridad de la señal con dos diferentes razones de muestreo. Las mediciones de ambos monitores han sido realizados con las mismas caraterísticas. El objetivo es ver el comportamiento de los monitores cuando la señal a verificar esta libre de falla y cuando presenta una violación de integridad de señal. Para lograr esto, se establece una frecuencia de muestreo coherente para cada frecuencia de señal a verificar. La frecuencia de muestreo escogida determina la ventana de prueba en la que se va a verificar la señal. En la resultante ventana de prueba la señal se repite M y serán tomadas N muestras. Si la señal a verificar es simétrica, esto es, 50% de ciclo útil, $\frac{N}{2}$ muestras serán tomadas en el estado bajo y alto. Para el caso libre de falla y si la señal se esta verificando en el estado alto, el monitor de estado alto es el que va producir información útil.

El monitor contiene dos nodos de salida que son complementarios en el fase de verificación de la señal. Llamemos OUTX a un nodo de salida y OUTXN al nodo complementario. En la primera mitad de la ventana de prueba se verifica se verifica el estado alto de la señal y la segunda mitad el estado bajo. A cada mitad de la ventana de prueba le corresponden $\frac{N}{2}$ muestras. Por ejemplo, si en la vetana de prueba se van a tomar 8 muestras, 4 muestras serán para la parte alta y 4 para la parte baja de la señal bajo prueba. Como la señal está libre de falla en la primera mitad de la ventana de prueba el nodo OUTX presentará 4 pulsos, mientras que el nodo OUTXN permanecerá en un estado bajo. En la segunda mitad de la ventana de prueba el nodo OUTX permanecerá en estado bajo, mientras que OUTXN presentará pulsos.

El caso con violación de integridad de señal se genera inyectandole a la señal un pulso de ruido en la parte lógica alta. En la primera mitad de la ventana de prueba se verifica la parte alta de la señal y en la segunda mitad la parte lógica baja. En las primeras 4 muestras no se obtienen 4 pulsos en el nodo OUTX puesto que el monitor de estado alto detecta una violación de integridad de señal. El número de pulsos ausentes está determinado por el número de muestras que se tomen al pulso de ruido. En la segunda mitad de la ventana de prueba el nodo OUTX no presenta pulsos, mientras que el nodo OUTXN presenta 4 pulsos. Mediciones experimentales semejantes fueron aplicadas para el monitor de estado bajo. La diferiencia consiste en que el pulso de ruido ahora es aplicado en el estado lógico bajo.

Las mediciones experimentales fueron repetidas para ambos monitores y cambiando la frecuencia de muestreo. Con esta frequencia de muestreo se toman 12 muestras en la ventana de prueba. Esto quiere decir que se esta aumentando la resolución del muestreo ya que más valores de la señal bajo verificación se están evaluando. Los resultados mostrados comprueban la funcionalidad de los monitores a diferentes frecuencias de muestreo. También se repiten las mediciones ahora cambiando la frecuencia de la señal a verificar a la frecuencia más alta obtenida en CI de prueba que es 917MHz.

El trabajo presentado a demostrado que la metodología propuesta para la verificación de integridad de la señal funciona correctamente. Los resultados experimentales validan los resultados de la simulación de la metodología. Podemos concluir que una solución para verificar undershoots y overshoots en señales digitales de alta velocidad se ha propuesto y validado por medio de mediciones experimentales en esta tesis.

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